A Novel mm-Wave Heterojunction JFET Technology with Suppressed Hole Injection

Final Progress Report

Dr. Umesh K. Mishra
Dr. Jeffrey B. Shealy

September 1996

U.S. Army Research Office

DAAH04-93-G-0033

University of California, Santa Barbara
Department of Electrical & Computer Engineering

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	September 1996	Final Progress (15 Jan 1993-14 Jan 1996)

4. TITLE AND SUBTITLE

A Novel mm-Wave Heterojunction JFET Technology With Suppressed Hole Injection

5. FUNDING NUMBERS

DAAH04-93-G-0033

6. AUTHOR(S)

Dr. Umesh K. Mishra
Dr. Jeffrey B. Shealy

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Department of Electrical & Computer Engineering
University of California
Santa Barbara, CA 93106

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 2709-2211

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ARO 31136.2-EL-SDI

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

We have developed a device technology using n-AlInAs/GaInAs on InP substrates, where the gate technology incorporates a p-n junction barrier. The p-n junction exists between an undepleted p-type surface layer (p^+-GaInAs) and the two-dimensional electron gas (2DEG) in the GaInAs channel. The p^+-2DEG junction provides a sufficiently high gate barrier that exhibits low gate leakage current and a high breakdown voltage. At the same time, the fixed gate-to-channel separation (solely determined by the MBE growth) leads to a reproducible gate barrier height, resulting in high threshold voltage uniformity ($\sigma(V_{th})$=13.7mV).

The junction barrier gate technology is the best choice of the three available gate technologies (namely insulator barrier gate, Schottky barrier gate, and the p-n junction barrier gate) for InP-based FETs. The low parasitic resistance and low gate leakage current produced state-of-the-art minimum noise figure (F_{min}) and associated gain (G_a) of 0.45 dB and 14.5 dB at 12GHz. The combination of reduced gatelength (0.2μm) and reduced parasitic transit delay translated into a unity gain cut-off frequency (f_τ) of 105 GHz. The low input resistance (due to high acceptor doping in the gate layer) and high $^{C_{gs}}/_{C_{gd}}$ ratio (due to a high aspect ratio design) of the JHEMT improved the unity power gain cut-off frequency (f_{max}) to 220 GHz. This is the highest f_{max} ever reported for a junction-barrier FET (JFET).

14. SUBJECT TERMS	15. NUMBER OF PAGES
p-n junction barrier; gate technology; JFET; JHEMT	182
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Development and Characterization of High Threshold Uniformity n-AlInAs/GaInAs Junction-Modulated HEMTs (JHEMTs)

Abstract

We have developed a device technology using n-AlInAs/GaInAs on InP substrates, where the gate technology incorporates a p-n junction barrier. The p-n junction exists between an undepleted p-type surface layer (p^+-GaInAs) and the two-dimensional electron gas (2DEG) in the GaInAs channel. The p^+-2DEG junction provides a sufficiently high gate barrier that exhibits low gate leakage current and a high breakdown voltage. At the same time, the fixed gate-to-channel separation (solely determined by the MBE growth) leads to a reproducible gate barrier height, resulting in high threshold voltage uniformity ($\sigma(V_{th})$=13.7mV).

The junction barrier gate technology is the best choice of the three available gate technologies (namely insulator barrier gate, Schottky barrier gate, and the p-n junction barrier gate) for InP-based FETs. The lack of a large bandgap insulator (with low interface states) in III-V materials eliminates the choice of an insulator barrier gate technology. Further, the InP-based Schottky-barrier gate technology is limited by (i) the weakly pinned, low Schottky barrier height (0.6eV) on AlInAs, and (ii) gate recess non-uniformities. The problems of gate contact resistance and hole injection associated with the junction barrier gate technology are addressed by very high acceptor doping ($1x10^{20}cm^{-3}$) and the large hole barrier provided by this material system.

The low parasitic resistance and low gate leakage current produced state-of-the-art minimum noise figure (F_{min}) and associated gain (G_a) of 0.45 dB and 14.5 dB at 12 GHz. The combination of reduced gatelength (0.2μm) and reduced parasitic transit delay translated into a unity gain cut-off frequency (f_τ) of 105 GHz. The low input resistance (due to high acceptor doping in the gate layer) and high C_{gs}/C_{gd} ratio (due to a high aspect ratio design) of the JHEMT improved the unity power gain cut-off frequency(f_{max}) to 220 GHz. This is the highest f_{max} ever reported for a junction-barrier FET (JFET).

Table of Contents

V. p^+-GaInAs/n-AlInAs/GaInAs JHEMTs

V. Conclusion

Appendices

Chapter 1
Introduction

1.1 Motivation

High electron mobility transistors based on the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ material system are attractive for low noise applications (e.g. Direct Broadcast Satellite (DBS), satellite communications, and radio astronomy) at microwave and millimeter-wave frequencies. The high average velocity ($v_{ave} > 2.0x10^7 \frac{cm}{sec}$)[1] in $Ga_{0.47}In_{0.53}As$ translates into short transit delays through the device. Further, the combination of high electron mobility ($\mu \approx 10{,}000 \frac{cm^2}{V \cdot sec}$)[2] and high sheet concentration ($n_s > 3x10^{12} cm^{-2}$)[3] allows low parasitic resistance. However, the performance (e.g. breakdown voltage, static power dissipation, and forward gate voltage swing) of the $Al_{0.48}In_{0.52}As/ Ga_{0.47}In_{0.53}As$ HEMT with a Schottky barrier gate (hereafter referred to as the Schottky HEMT) is limited by the low Schottky barrier height of metal on $Al_{0.48}In_{0.52}As$ (0.6eV)[4]. Furthermore, the manufacturability of the Schottky HEMT is restricted by the lack of a reproducible gate technology. For convenience, the alloy composition numbers are hereafter omitted and, unless otherwise stated, the composition is assumed to be lattice matched.

First, the low Schottky barrier height of metal on AlInAs permits electron injection from the gate into the channel under reverse bias (see Figure 1.1a). These injected electrons contribute to the reverse

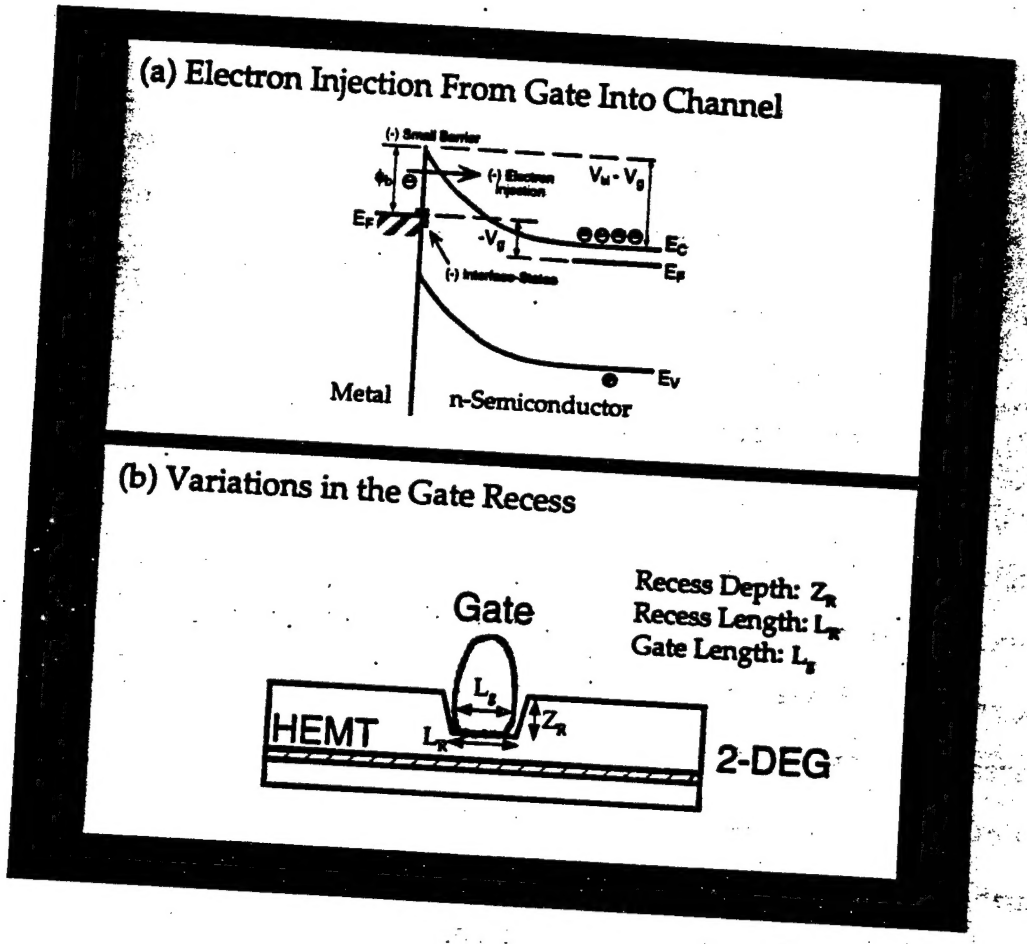


Figure 1.1. Limitations of the Schottky HEMT technology: **(a)** electron injection from the gate into the channel which leads to excessive gate leakage current, and **(b)** variations in the gate recess which causes deviations in threshold voltage, input impedance, and output conductance.

leakage current observed in the diode characteristics of AlInAs/GaInAs Schottky HEMTs. The off-state breakdown in the AlInAs/GaInAs Schottky HEMT is determined[5] by the number of injected electrons which experience impact ionization in the high field region of the channel. The on-state breakdown is determined by current multiplication either in the channel or at the drain contact. Therefore, it is desirable to (i) minimize the injection of electrons from the gate into the channel, and (ii) reduce the electric field near the drain electrode to suppress impact ionization.

Second, the gate recess length and depth (see Figure 1.1b) of the Schottky HEMT determine (i) the threshold voltage, (ii) input impedance (e.g. C_{gs}), (iii) the electric field profile surrounding the gate, and (iv) the output conductance, G_{ds} (which influences the minimum noise figure, F_{min}[6]). Therefore, to obtain similar device characteristics across a wafer, the etch process used to define the gate recess trench must be uniform. The horizontal and vertical variations in the recess etch of the Schottky HEMT *prevent* (i) high threshold voltage uniformity, (ii) reproducible state-of-the art noise performance, and (iii) the maturation of a high yield, low cost MMIC technology. Therefore, it is desirable to develop a reproducible gate technology compatible with the AlInAs/GaInAs HEMT structure.

1.2 Approach: The Junction Modulated HEMT (JHEMT)

In order to improve the gate technology, we have added

undepleted p^+ surface layers to enhance the gate barrier (reducing electron injection from the gate into the channel) and to provide a reproducible gate potential (improving the threshold voltage uniformity). To improve the breakdown characteristics, we have regrown n^+ channel contacts using MOCVD to reduce the electric field near the drain electrode (by increasing the electron collection area) and to reduce the minority carrier population in the drain region (preventing hole injection from the drain metal).

In contrast to a conventional Schottky HEMT (hereafter called the HEMT), the junction HEMT (JHEMT) utilizes a highly doped p^+-region, forming a p-n junction barrier to modulate the 2-DEG. The effect of this additional surface layer on the energy band diagram is seen in Figure 1.2, where the energy band diagrams of a typical HEMT and JHEMT are shown. The electron energy barrier in the HEMT is simply the Schottky barrier height of the gate metal on the AlInAs barrier layer (0.6eV). In the case of the JHEMT, the electron barrier height is the built-in potential of the p-2DEG junction, which may be as high as the bandgap of the gate material (1.4eV, for p^+-AlInAs). With the exception of the additional p-type surface layer, the JHEMT is identical (as far as the structure is concerned) to the HEMT.

Since the HEMT and JHEMT channel structures are virtually identical, the electron transport characteristics in the channel are expected to be very similar. A plot of electron mobility versus sheet electron concentration comparing the electron mobility of InP-Based

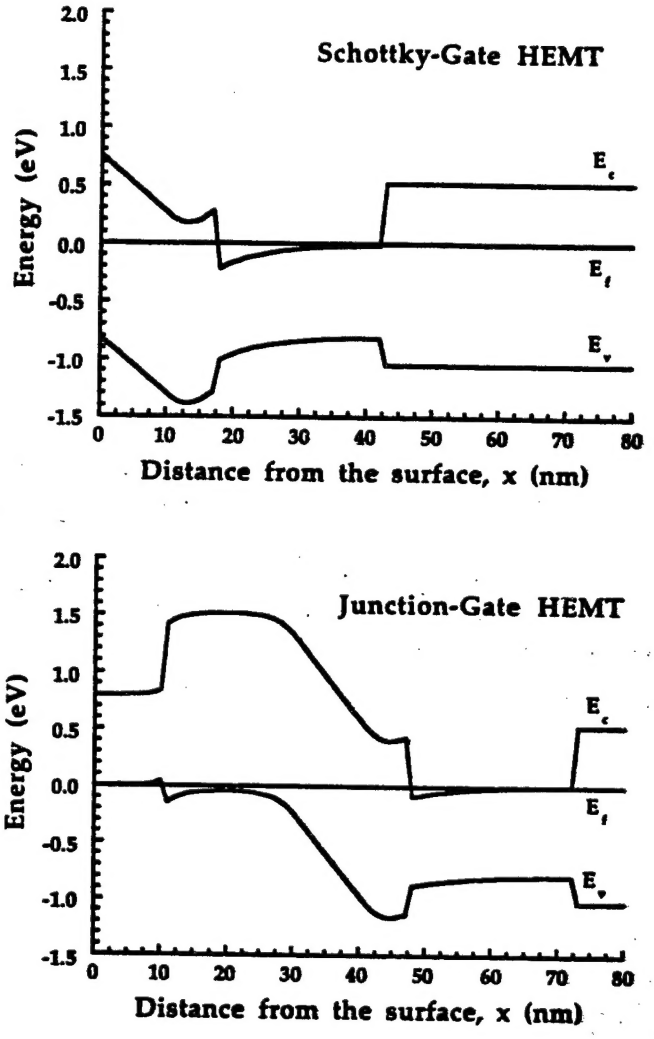


Figure 1.2. Energy band diagram comparison of the HEMT (top) and the JHEMT (bottom). The effective Schottky barrier height for the HEMT is controlled by surface interface states. The effective electron barrier of the JHEMT is determined by built-in potential of the gate diode whose maximum is the energy bandgap of the p-type material.

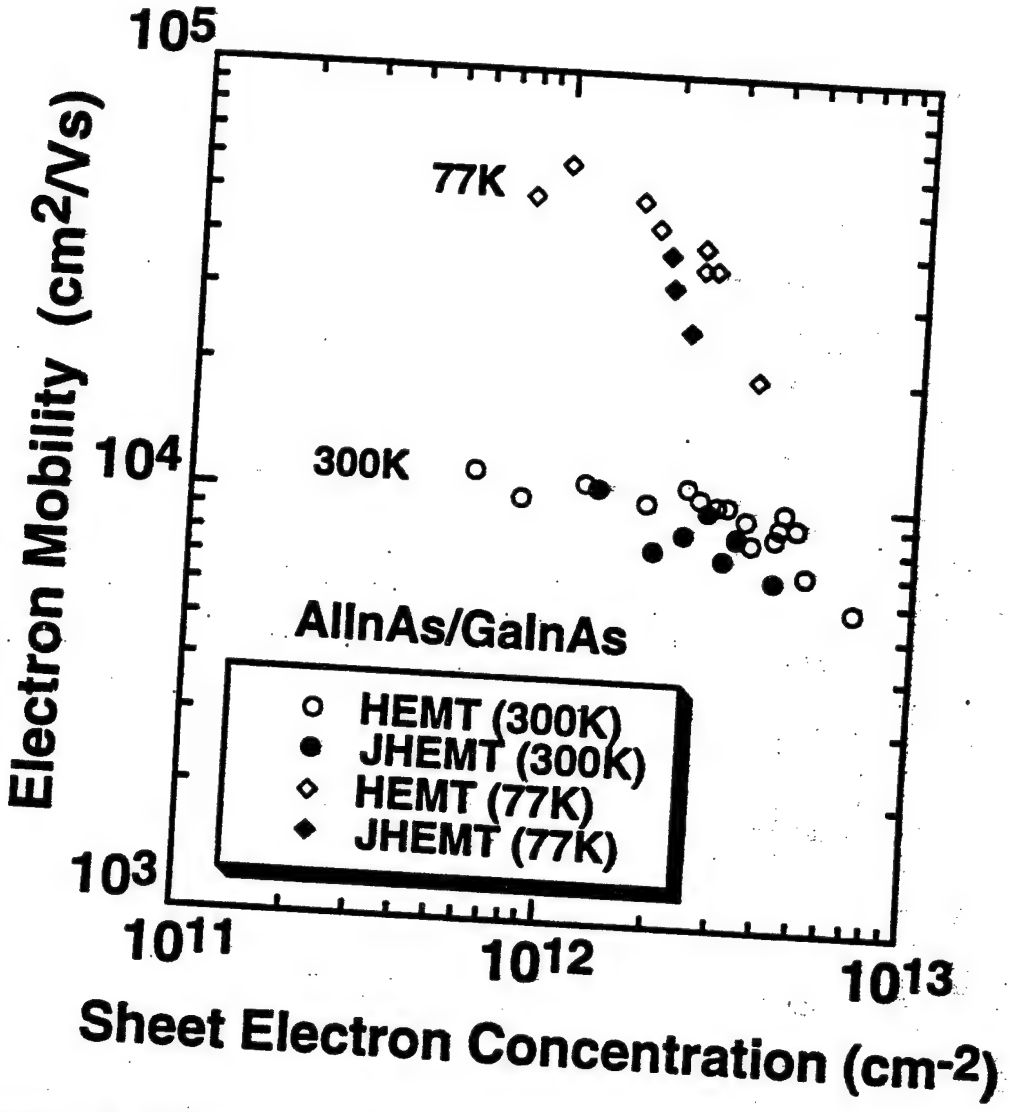


Figure 1.3. Comparison of electron mobility of the HEMT and the JHEMT. As expected, the similar mobilities indicate the excellent transport properties of the HEMT structure are attained in the JHEMT structure. (For HEMT references: see [7])

JHEMTs (fabricated in this work) to HEMTs is given in Figure 1.3. This data proves that the electron transport characteristics in the channel do not suffer by the addition of p^+-layers to the surface.

The fabrication of the HEMT and the JHEMT require, in principle, the same processing steps with the exception of the gate recess etch. In the HEMT, a gate recess etch occurs after the gate lithography and prior to gate metal deposition. The purpose of the gate recess etch in the HEMT is i) to reduce the gate-to-channel spacing by etching *into* the barrier layer, increasing both the intrinsic gate capacitance (relative to extrinsic capacitance) and the aspect ratio (L_g/d_{p-2DEG}) of the device and ii) to adjust the threshold voltage. In contrast, the gate recess etch of the JHEMT (which is actually a recess etch of the access regions) occurs after both the gate lithography and gate metallization. The purpose of the gate recess in the JHEMT is i) to define the physical footprint of the gate, which determines the effective gatelength, and ii) to reduce the sheet resistance in the access regions[8], effectively lowering the source and drain parasitic resistance. Thus, the purpose of the gate recess etch is fundamentally different in the two devices as shown from the schematic in Figure 1.4.

The JHEMT offers an alternative means to obtain threshold voltage uniformity. Uniformity in the gate region of the JHEMT results from the opposite order (relative to the HEMT fabrication process) in which the recess etch step and gate metallization steps occur. The threshold voltage has either a linear or quadratic

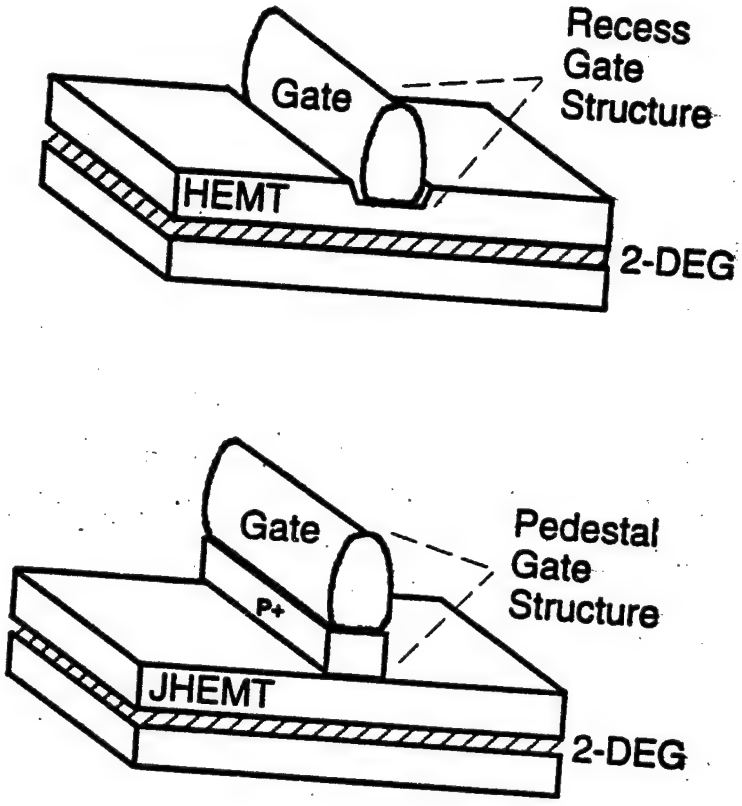


Figure 1.4. Comparison of the gate structures in the HEMT (top) and the JHEMT (bottom). The HEMT structure consists of a recess gate structure whereas the JHEMT has a pedestal gate structure. The subtle differences in the gate structures have significant impact on threshold voltage uniformity as shown in Chapter 2.

relationship with respect to the gate-to-channel separation[9], depending on the doping scheme used in the upper donor layer. Recall for the HEMT, one purpose of the recess etch is to control threshold voltage. Therefore, non-uniformities in the recess etch depth result directly in threshold voltage variations. Conventionally, the two approaches for obtaining threshold voltage uniformity in HEMTs are selective wet chemical etching[10] and dry etching[11,12]. By comparison, the equivalent to the gate recess etch (in the JHEMT) occurs after the gate metal is deposited, and the distance from the gate to the channel remains unaltered by the recess etch step. Consequently, the gate-to-channel separation remains fixed, resulting in high threshold voltage uniformity.

In addition to the modification to the gate structure, the channel contact regions are replaced with n^+ GaInAs regrown by MOCVD. The concept of regrown contacts to a 2-DEG has previously been reported[13]. The n^+ contacts reduce the electric field in the channel near the drain electrode (by increasing the area of electron collection) and suppress hole injection from the metal into the channel (due to low minority carrier population in the n^+ contact region). Experimentally, both the on-state and off-state breakdown voltage in the GaInAs channel JHEMT are enhanced as discussed in Chapter 4.

1.3 Historical Background

1.3.1 Modulation Doping and the InP High Electron Mobility Transistor

The concept of *Modulation doping*[14] is now explained as applied to the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ heterojunction. Donor impurities are selectively introduced in the large bandgap material ($Al_{0.48}In_{0.52}As$) near the hetero-interface. The larger bandgap and smaller electron affinity of AlInAs compared to GaInAs provides a conduction band energy discontinuity, ΔE_c, at the hetero-interface. This energy difference allows free electrons in the AlInAs donor layer to diffuse into the GaInAs layer to form the conducting channel. The slope of the conduction band edge at the hetero-interface is such that any electrons which diffuse into channel region are pulled back toward the donor layer. However, they are prevented from re-entering the donor layer and neutralizing their uncompensated parent atoms by the conduction band discontinuity, ΔE_c, which acts as a confining potential. Consequently, both the supply of electrons (donor density) and the magnitude of ΔE_c determine the maximum 2-DEG concentration in the channel. The modulation-doped $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ hetero-structure is grown lattice matched to InP ($a_o = 5.85\text{Å}$, see Figure 1.5).

The complete InP HEMT structure is shown in Figure 1.6. The current carrying active layer (hereafter called the channel) consists of a thin (typically 15-40nm) epitaxial-layer of high-purity GaInAs. Above this active layer is an undoped AlInAs *spacer layer* (employed to reduce remote coulombic scattering and whose thickness is optimally 2-5nm) followed by a selectively doped n-type (e.g. Si:$1x10^{19}cm^{-3}$)

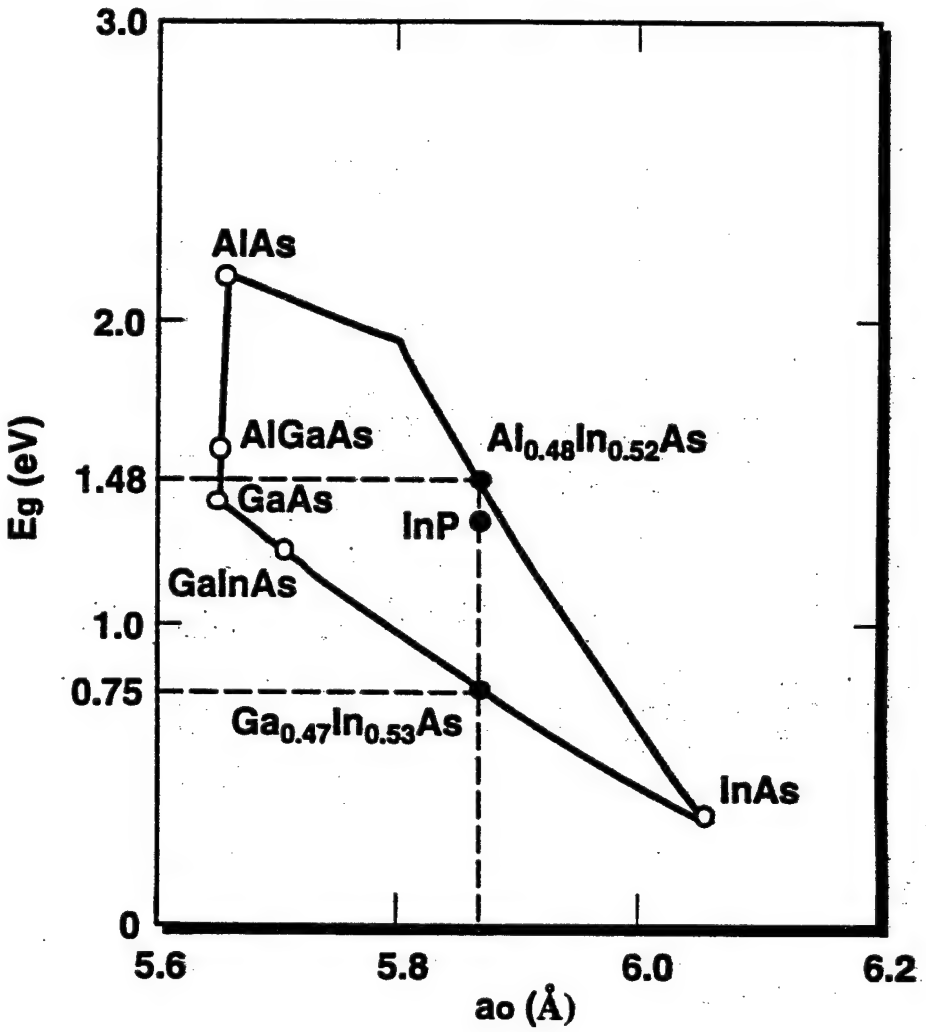


Figure 1.5. Energy Gap versus Lattice Constant for various materials. The lattice constant of InP is 5.85Å. (Reference [15])

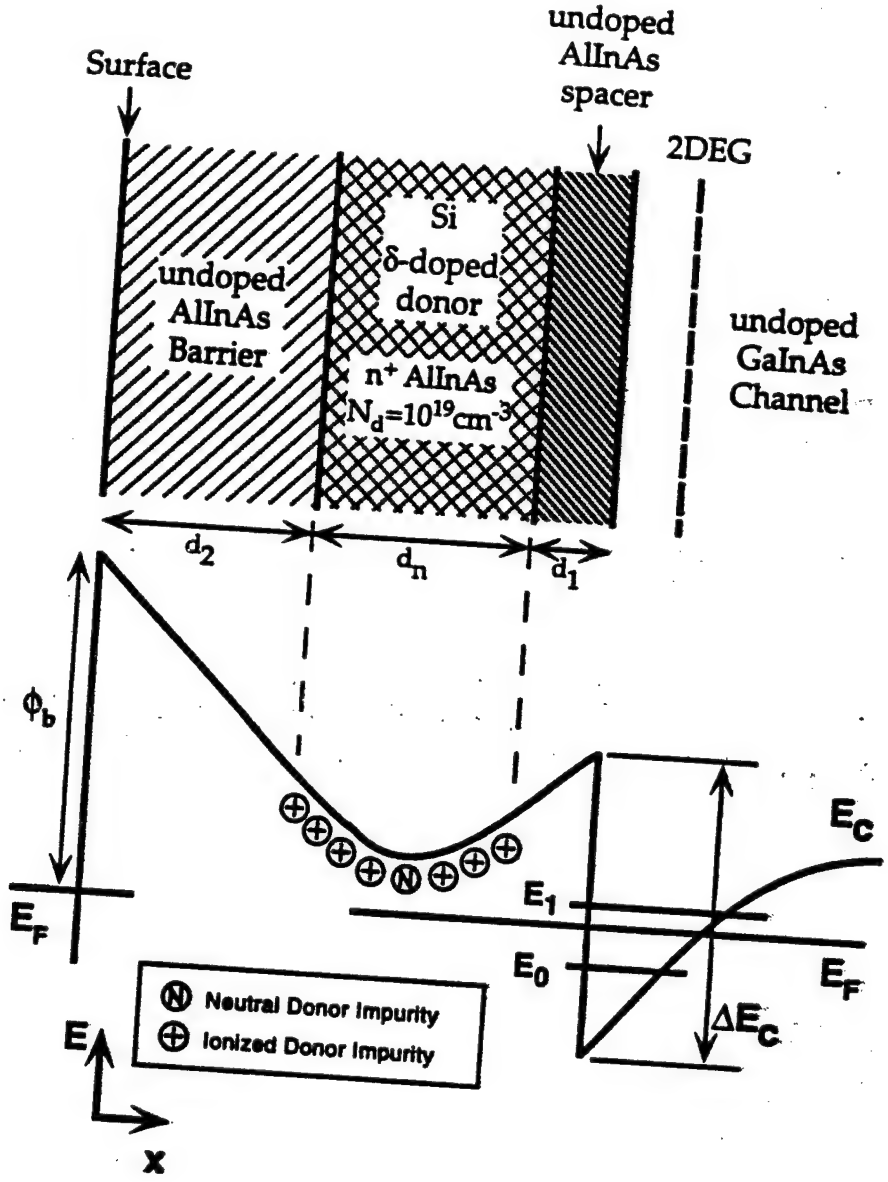


Figure 1.3. Modulation-doped AlInAs/GaInAs HEMT structure and associated conduction energy band diagram. The thin n+-GaInAs contact layer is not shown for simplicity.

AlInAs *donor layer*. Finally, an undoped AlInAs Schottky *barrier layer* followed by a thin *contact layer* is grown above the donor layer to complete the HEMT structure.

The electrons in the undoped GaInAs channel layer are spatially separated from their parent donor atoms. Therefore, ionized impurity scattering is minimized (especially at low temperatures) and the electrons moving in an applied electric field (parallel to the AlInAs/GaInAs hetero-interface) attain high carrier mobility approaching the maximum possible for undoped GaInAs. The mobility of the AlInAs/GaInAs HEMT at 300K and 77K is 10,000 and 60,000 cm^2/V_{sec}, respectively (see Figure 1.3). The enhancement factor of electron mobility of a HEMT over a GaInAs doped-channel ($n=1x10^{18}cm^{-3}$) FET is 2 and 10 at 300K and 77K, respectively[16]. The higher enhancement factor at 77K is because ionized-impurity scattering is the transport-limiting mechanism, whereas at 300K, polar optical phonon scattering is a competing mechanism.

1.3.2 Evolution of the InP HEMT

The concept of modulation doping along with the advanced material growth technique of Molecular Beam Epitaxy (MBE) led to the Schottky-barrier gate, modulation-doped n-AlGaAs/GaAs hetero-structure transistors in the early 1980's[17,18,19,20]. As a result, the names high electron mobility transistor (HEMT), selectively-doped heterojunction transistor (SDHT), two-dimensional electron gas field

effect transistor (TEGFET), and modulation-doped field effect transistor (MODFET) were adopted, signifying the underlying physics of the devices[21].

In 1983, Eastman suggested the development of modulation-doped $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ hetero-structure on InP as a promising candidate for high speed devices[22]. The lattice-matched $Ga_{0.47}In_{0.53}As$ alloy on InP possesses three distinct advantages over the lower indium mole-fraction $AlGaAs/Ga_{1-x}In_xAs$ PHEMT. First, the higher ΔE_C (0.5eV)[23] translates into higher 2-DEG concentration and higher modulation efficiency[24]. Second, the lower electron effective mass (m_e^*) results in higher electron mobility (μ_e>10,000 cm^2/Vs). Finally, the higher average velocity in the channel (>2.0×10^7 cm/s) reduces the electron transit time through the device[25]. The combination of high electron mobility and high 2-DEG concentration result in lower channel resistivity.

In 1985, Professor Eastman's group at Cornell University reported[26] the first $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ HEMT lattice-matched to an InP substrate[27]. Thereafter, several research labs began investigating AlInAs/GaInAs HEMTs on InP substrates (see for example [28,29,30]). By the summer of 1988, Mishra *et al.* at Hughes Research Laboratories reported a unity current gain cut-off frequency[31], f_T, of 170 GHz utilizing a 0.1 μm gatelength AlInAs/GaInAs HEMT[32]. This work clearly demonstrated the superior properties of modulation-doped AlInAs/GaInAs heterojunctions on InP. In addition, the results

were significant because they far exceeded the performance of published 0.1 μm gatelength AlGaAs/GaAs HEMTs[33]. By the end of 1988, Mishra *et al.* improved the f_T to over 200 GHz[34] by increasing the In mole-fraction in $Ga_{1-x}In_xAs$ ($x = 0.62$), further reducing the electron effective mass. One year later, a drastic reduction of the parasitic resistance, R_s+R_d, was achieved by self-aligning the ohmic contacts to a mushroom-shaped gate metal[35]. The reduced parasitic time delay resulted in a record value of over 250 GHz (f_T).

Nguyen *et al.* at Hughes Research Laboratories further improved the device performance by i) optimization of $Ga_{1-x}In_xAs$ ($x = 0.80$) as the channel material, ii) further reduction in parasitic resistance, and iii) successful reduction of the gatelength to 50 nm[36]. These improvements advanced the state-of-the-art cut-off frequency to 340 GHz (f_T)[37]. Since 1992, two other groups have reported 300 GHz (f_T) Schottky-gate HEMT device performance[38,39]. Due to the high electron velocity and the low parasitic resistance, the HEMT is the fastest three-terminal device in the world and will probably remain so for some time to come.

1.4 Synopsis

The principal objective of this dissertation is to establish a body of knowledge governing the design of high performance and high uniformity lattice-matched n-AlInAs/GaInAs junction HEMTs (JHEMTs) for microwave and millimeter wave applications. In Chapter 2, the design aspects of the gate and access regions of the JHEMT are examined. The Lever Rule relation is derived for purposes of designing the barrier, donor, and spacer layers. Next, the utilization of surface layers to increase the Schottky barrier height is discussed and the advantages of the p-n junction as the gate electrode of the HEMT are presented. Thereafter, an accurate threshold voltage model is developed. Finally, a lumped element approximation of the JHEMT input impedance is used to attain an equivalent circuit model for the device.

Chapter 3 discusses the regrowth of ohmic contacts by MOCVD. Next, the fabrication process of the mm-Wave JHEMT is presented and the ohmic contact technologies available (alloyed versus regrown) to fabricate the JHEMT are examined. Finally, the method utilized to characterize the electronic transport properties of the JHEMT is presented.

Chapter 4 describes the performance of single-doped p+-AlInAs/n-AlInAs/GaInAs JHEMTs with gatelengths of 1μm and 0.2μm. The on-state and off-state breakdown voltages are directly compared for 1μm gatelength devices with both regrown and alloyed

contacts.

Chapter 5 details the DC and RF performance of the single- and double-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT with gatelengths of 0.2μm and 0.15μm, respectively[40]. In particular, the threshold voltage uniformity is examined along with the influence of the barrier layer thickness on the threshold voltage. A one-dimensional transport model is presented to predict the forward current in the gate diode. The results suggest that the forward current in the p^+-GaInAs/n-AlInAs/GaInAs JHEMT is dominated by tunneling through the AlInAs barrier layer and not by thermionic emission over the barrier.

Chapter 6 summarizes the most important findings in this investigation and presents a few suggestions for future work in the area of InP-based JHEMTs. Appendix A contains the derivation of the lumped-element model for the JHEMT input impedance discussed in Chapter 2. Next, Appendix B presents the doping concentration as a function of flow rate obtained in the MOCVD reactor used to regrow the ohmic contacts. Then, Appendix C gives a detailed process traveler of the mm-Wave JHEMT process. Appendix D contains a plot of depletion depth versus doping for a given surface potential. Appendix E contains the HP basic program written by this author to calculate the gate-diode current in the JHEMT. Appendix F contains the bias dependent model parameters of the double-doped JHEMT with various gatelengths (0.15, 0.33, and 0.48μm).

References

[1] See For Example: L.D. Nguyen, A.S. Brown, M.A. Thompson, and L.M. Jelloian, "50-nm Self-Aligned-Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," IEEE Trans on Electron Dev., Vol 39, No. 9, Sept. 1992.

[2] See For Example: U.K. Mishra, L.M. Jelloian, M. Lui, and M.A. Thompson, S.E. Rosenbaum, and K.W. Kim, "Effect of n and p channel doping on the I-V characteristics of AlInAs-GaInAS HEMTs," GaAs and Related Compounds, pp. 287-293, 1991.

[3] See For Example: U.K. Mishra, A.S. Brown, L.M. Jelloian, L.H. Hacket, and M.J. Delaney, "High Performance Submicrometer AlInAs-GaInAs HEMTs," IEEE Electron Dev. Lett., Vol 9, pp. 41-43, 1988.

[4] L.P. Sadwick, C.W. Kim, K.L. Tan, and D.C. Streit, "Schottky Barrier Heights of n-Type and p-Type $Al_{0.48}In_{0.52}As$," IEEE Elect. Dev. Lett:, Vol. 42, No. 11, pp 626-628, Nov. 1991.

[5] S.R. Bahl, J.A. del Alamo, J. Dickman, and S. Schildberg, "Off-State Breadown in InAlAs/InGaAs MODFETs," IEEE Trans. Elect. Dev., Vol. 42, No.1, Jan 1995.

[6] M.W. Pospieszalski, "Model of Noise Parameters of MESFET's and MODFET's and their Frequency and Temperature Dependence," IEEE Trans. Microwave Theory Tech., Vol. 37, pp. 1340-1350, Sept. 1989.

[7] See F. Ali and A. Gupta, "HEMTs and HBTs: Devices, Fabrication, and Circuits," Artech House, 1991, p. 130

[8] The access regions are defined as the regions which access the intrinsic device, not including the ohmic contact resitance. The sheet resistance in these regions is high due to the high surface potential when the p+ region is present.

[9] G-W Wang and L.F. Eastman, "An Analytical Model for I-V and Small-Signal Characteristics of Planar-Doped HEMTs," IEEE Trans. on MTT, Vol. 37, pp. 1395-1400, Sept 1989.

[10] M. Tong, K. Nummila, A. Ketterson, I. Adesida, C. Caneau, and R. Bhat, "InAlAs/InGaAs/InP MODFET's with Uniform Threshold Voltage Obtained by Selective Wet Gate Recess," IEEE Electron Dev. Lett., Vol. 13, No. 10. Oct. 1992.

[11] T. Aigo, A. Jono, A. Tachikawa, R. Hiratsuka, and A. Moritani, "High uniformity of threshold voltage for GaAs/AlGaAs high electron mobility transistors grown on a Si substrate," Appl. Phys. Lett. Vol. 64, No. 23, June 6 1994.

[12] H. Ishikawa, H. Shibata, and M. Kamada, "Excellent Uniformity of threshold voltage of Si-planar-doped AlInAs/GaInAs heterointerface field-effect transistors grown by metalorganic chemical vapor deposition," Apply. Phys. Lett., Vol. 57, No. 5, July 30 1994.

[13] A. Palevski, P. Solomon, T.F. Kuech, and M.A. Tischler, "Regrowth to a Two-Dimensiona Electron Gas", Appl. Phys. Lett., Vol. 56, 171, January 1990.

[14] R. Dingle H.L. Stormer, A.C. Gossard, and W. Wiegmann, "Electron Mobilities in Modulation-doped Semiconductor Heterojunction Superlattices," Appl. Phys. Lett., Vol. 33, pp. 665-667, Oct. 1978.

[15] A. Gupta, "High Electron Mobility Transistors for millimeter-wave and high speed digital IC applications," SPIE, Vol. 795, pp. 68-90, 1987.

[16] K.Y. Cheng, and A.Y. Cho, "Silicon Doping and Impurity Profiles in $Ga_{0.47}In_{0.53}As$ and $Al_{0.48}In_{0.52}As$ Grown by Molecular Beam Epitaxy," J. Appl. Phys., Vol. 53, No. 6,

June 1982.

[17] H.L. Stormer, R. Dingle, A.C. Gossard, and W. Wiegmann, and M.D. Sturge, "Two-Dimensional Electron gas at a Semiconductor-Semiconductor Interface," Solid-State Comm., Vol. 29, pp.705-709, 1979.

[18] K. Ohata, H. Hida, and H. Miyamoto, "A low-noise AlGaAs/GaAs FET with P+ Gate and Selectively Doped Structure," in IEEE Int. MTT-S Microwave Symp. Dig., pp. 434-436, 1984.

[19] T. Mochizuki, H. Hinma, K. Handa, W. Akinaga, and K. Ohata, "Low-noise amplifiers using two-dimensional electron gas FETs," in IEEE Int. MTT-S Microwave Symp. Dig., pp. 543-546, 1985.

[20] D. Delagebeaudeuf and N.T. Linh, "Metal-(n)AlGaAs-GaAs two-dimensional electron gas FET," IEEE Trans. Electron Devices, Vol. ED-29, pp 955-960, June 1982.

[21] However, only the the names HEMT, MODFET, and more recently HFET remain popular acronyms used in recently published literature.

[22] L.F. Eastman, "Use of Molecular Beam Epitaxy in Research and Development of Selected High Speed Compound Semiconductor Devices," J. Vac. Sci. Technol. B 1 (2), pp. 131-134, Apr.-June 1983.

[23] R. People, K.W. Wecht, K. Alavi, and A.Y. Cho, "Measurement of the Conduction-Band Discontinuity of Molecular-Beam Epitaxial Growth of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Heterojunction by C-V Profiling," Appl.Phys. Lett., Vol. 43, pp. 118-120, 1983.

[24] M. C. Foisy, P.J. Tasker, B. Hughes, and L.F. Eastman, "The role of inefficient charge modulation in limiting the current-gain cutoff frequency of the MODFET," IEEE Trans Electron Dev., Vol ED35, pp. 871-878, July 1988.

[25] By comparison, a N-$Al_{0.30}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ PHEMT (on GaAs) has ΔE_c =0.42eV, μ_e=6000 cm^2/Vs and $V_{peak}=2x10^7$ cm/s (values taken from L.D. Nguyen, Ph.D. dissertation, Cornell Univ. Ithaca, NY, 1989).

[26] T. Itoh, A.S. Brown, L.H. Camnitz, G.W. Wicks, J.D. Berry, and L.F. Eastman, "A Recessed Gate $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ Modulation-Doped Field Effect Transistor," in Proc. IEEE/Cornell Conf. on Advanced Concepts in High Speed Semiconductor Devices and Circuits, pp. 92-101, 1985.

[27] In the same year, the tensile-strained, "pseudomorphic" $Ga_{1-X}In_XAs$ channel HEMT was being developed on GaAs(see for example J.J. Rosenburg, N. Benlamri, P.D. Kirchner, J.M. Woodall, and G.D. Pettit, " An $In_{0.15}Ga_{0.85}As/GaAs$ Pseudomorphic Single Quantum Well HEMT," IEEE Electron Dev. Lett., Vol. EDL-6, pp. 491-493, 1985). The device was eventually called the pseudomorphic HEMT, or simply PHEMT.

[28] C.K. Peng, M. I. Aksun, A. Ketterson, H. Morkoc, and K. Gleason, "Microwave Performance of InAlAs/InGaAS/InP MODFETs," IEEE Electron Dev. Lett., Vol EDL-8, pp. 24-26, 1987.

[29] A.S. Brown, U.K. Mishra, J.A. Henige, and M. Delaney, " The Impact of Epitaxial Layer Design and Quality on GaInAs/AlInAs High-Electron-Mobility Transistor Performance," J. Vac. Sci. Tech., Vol B6, No. 2, Mar./April 1988.

[30] A. Fatimulla, J. Abrahams, T. Laughran, and H. Heir, "High Performance InAlAs/InGaAs HEMTs and MESFETs," IEEE Electron Dev. Lett., Vol EDL-9, pp. 328-330, 1988.

[31] The unity current gain cut-off frequency is a useful figure-of-merit representing the

"speed" of the device. Recall, it is inversely-proportionial to the electron transit time through the device.

[32] U.K. Mishra, A.S. Brown, S.E. Rosenbaum, C.E. Hooper, M.W. Pierce, M.J. Delaney, S. Vaughn, and K. White, "Microwave performance of AlInAs-GaInAs HEMT's with 0.2 and 0.1μm gatelength," IEEE Electron Device Lett., Vol. 9, pp. 647-649, Dec. 1988.

[33] A.N. Lepore, M. Levy, R. Tiberio, P. Tasker, H. Lee, E. Wolf, L. Eastman, and E. Kohn, "0.1-μm gatelength MODFETs with unity current gain cut-off frequency above 110GHz," Electron Lett., Vol. 24, No. 6, pp.364-366, Mar. 17, 1988.

[34] U.K. Mishra, A.S. Brown, and S.E. Rosenbaum, " DC and RF performance of 0.1-μm gatelength $Al_{0.48}In_{0.52}As/Ga_{0.38}In_{0.62}As$ pseudomorphic HEMTs," in IEDM's Tech. Dig., pp.180-183, Dec. 1988.

[35] U.K. Mishra, A.S. Brown, L.M. Jelloian, M. Thompson, L.D. Nguyen, and S.E. Rosenbaum, " Novel High Performance Self-Aligned 0.1μm long T-gate AlInAs-GaInAs HEMTs," in IEDM's Tech. Dig., pp. 101-104, Dec. 1989.

[36] Successive reduction in gatelength to 80nm and 65nm gatelength was achieved before the 50nm device was reported, The interested reader is directed to the following 2 articles for more thorough account of the development of the 50nm gatelength device.

•L.D. Nguyen, L.M. Jelloian, M.A. Thompson, and M. Lui, "Fabrication of a 80-nm self-aligned T-gate AlInAs/GaInAs HEMT", IEDM Tech. Dig., Dec. 1990.

•L.D. Nguyen, A.S. Brown, M.A. Thompson, L.M. Jelloian, L.E. Larson, and M. Matloubian, "650Å Self-Aligned Pseudomorphic $Al_{0.48}In_{0.52}As/Ga_{0.20}In_{0.80}As$ High Electron Mobility Transistor", IEEE Electron Dev. Lett., Vol. 13, No. 3, March 1992.

[37] L.D. Nguyen, A.S. Brown, M.A. Thompson, and L.M. Jelloian, "50-nm Self-Aligned-Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," IEEE Trans on Electron Dev., Vol 39, No. 9, Sept. 1992.

[38] T. Enoki, M. Tomizawa, Y Umeda, and Y. Ishii, "0.05-μm-gate InAlAs/InGaAs High Electron Mobility Transistor and Reduction of its Short Channel Effects," Jpn. J. Appl. Phys. Part 1, Vol. 33, pp.798-803, Jan. 1994 .

[39] M. Wojtowicz, R. Lai, D.C. Striet, G.I. Ng, T.R. Block, K.L. Tan, P.H. Liu, A.K. Freudenthal, and R.M. Dia, "0.1μm Graded InGaAs Channel InP HEMT with 305GHz f_t and 340GHz f_{max}," IEEE Electron Dev. Lett., Vol.15, No. 11, November 1994.

[40] Note: for the remainder of this dissertation, devices with gatelength of 0.2μm are referred to as 0.2μm gatelength devices.

Chapter 2
Design of mm-wave JHEMTs

A cross section of the p^+-GaInAs/n-AlInAs/GaInAs JHEMT is shown in Figure 2.1. The device may be divided into two regions: the *gate region* (immediately under the gate metal) and the *access regions* (between the gate and the ohmic contacts). The two regions have different surface potentials as shown in the associated band diagrams. To achieve a high performance device, both regions must be effectively designed.

The design of mm-Wave JHEMTs begins with a derivation of the *Lever Rule* which governs the transfer of electrons from the donor layer to the channel. Second, the design criteria pertaining to the access regions are discussed. Next, a one-dimensional threshold voltage model is fully developed. Afterwards, a lumped-element approximation for the input impedance of the JHEMT is derived. Finally, the five design philosophies of the gate region are presented.

2.1 The *Lever Rule* Layer Design Model

The *Lever Rule* model[1] dictates the distribution of electrons in a modulation-doped heterostructure. Given knowledge about the (δ-doped) donor layer, the model provides guidance when choosing the thicknesses of the spacer layer and barrier layer required to achieve a certain electron concentration in the channel. The model assumes

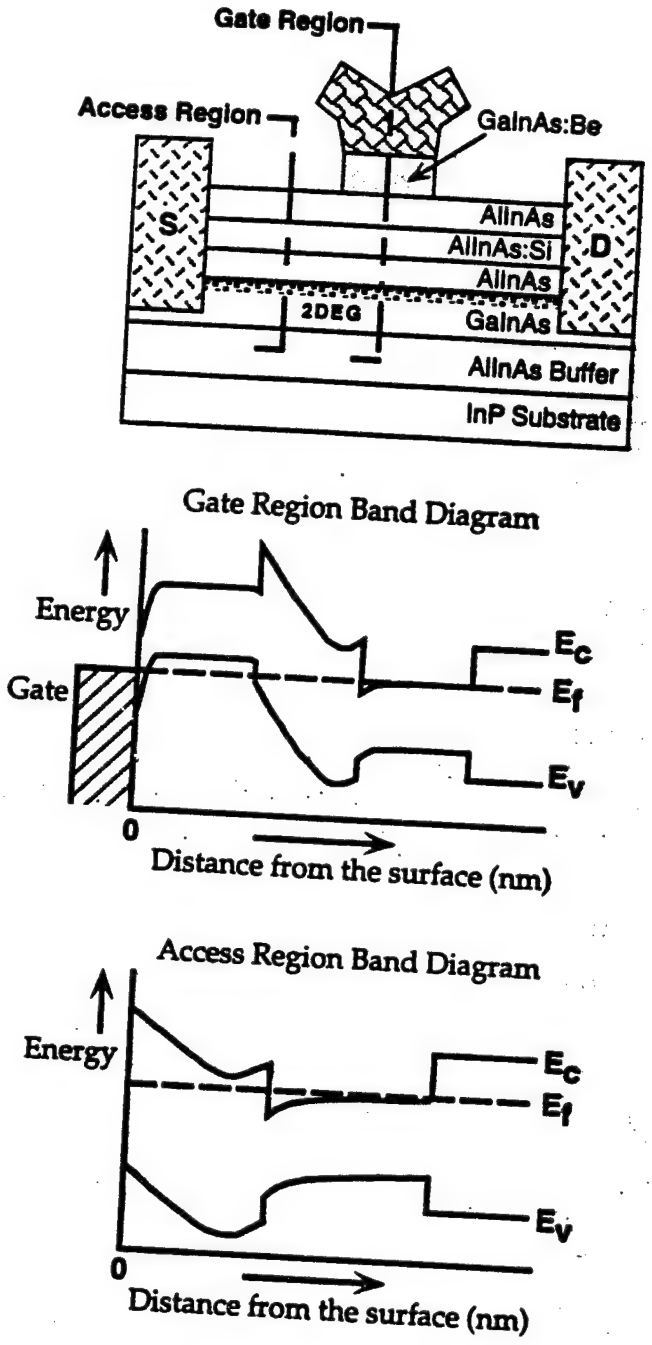


Figure 2.1. Cross-section of the p+-GaInAs/n-AlInAs/GaInAs JHEMT defining the gate and access regions. The associated band diagrams of these regions are also shown.

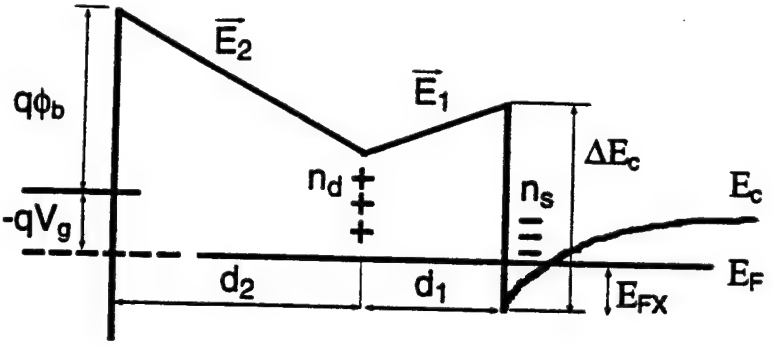


Figure 2.2. Energy band diagram of the modulation-doped AlInAs/GaInAs heterojunction used to derive the Lever Rule.

only that the donor impurities are fully ionized.

The modulation-doped band structure for the model is given in Figure 2.2. The thicknesses d_2 and d_1 are the thicknesses of the barrier and spacer layers, respectively. The sheet electron concentrations n_d and n_s are electron concentrations in the donor and channel layer, respectively. ϕ_b is the Schottky barrier height on the wide-bandgap material (e.g. AlInAs), and ΔE_C is the conduction band discontinuity at the heterojunction as defined in Chapter 1. The value E_{FX} is the distance from the conduction band edge at the hetero-interface to the Fermi level as shown in the figure. Lee and coworkers[2] have shown that E_{FX} may be given by the following linear approximation[3]:

$$E_{FX} = \Delta E_{FO}(\mathrm{T}) + a \cdot n_s \qquad [2.1]$$

where:

$\Delta E_{FO}(\mathrm{T})$ is the zero-intercept of the linearized $E_{FX}(n_s)$

function. note: $\Delta E_{FO}(300K) = 0$

a is the slope of the linearized $E_{FX}(n_s)$ function.

n_s is the 2-DEG concentration.

The rest of the analysis comes from applying Poisson's equation and Gauss' Law to the band structure. The electric field, E_1, may be written as:

$$E_1 = \frac{q \cdot n_s}{\varepsilon_2} \qquad [2.2]$$

where ε_2 is the dielectric constant in the large bandgap material (e.g. AlInAs). At T=300K, the potentials in the structure at 300K may be summed to obtain the following equation which may be solved exactly:

$$-V_g + \frac{\Phi_b}{q} - E_2 \cdot d_2 + E_1 \cdot d_1 - \frac{\Delta E_c}{q} + an_s = 0 \qquad [2.3]$$

An approximate solution in the case of the AlInAs system is obtained by recognizing that:

$$\frac{\Phi_b}{q} + an_s \approx \frac{\Delta E_c}{q} \qquad [2.4]$$

This estimate is good for AlInAs/GaInAs since Φ_b=0.6eV, ΔE_c=0.52eV, and an_s=0.20eV for $n_s = 1x10^{12} cm^{-2}$. The error in this approximation increases with n_s, but even at high channel concentrations, say $3x10^{12} cm^{-2}$, the approximation (equation [2.4]) is still acceptable. With the help of equation [2.4], equation [2.3] may be re-written (for the case when $V_g = 0$) as:

$$E_2 \cdot d_2 = E_1 \cdot d_1 \qquad [2.5]$$

Substituting equation [2.2] into [2.5]:

$$E_2 \cdot d_2 = \frac{qn_s}{\varepsilon_2} \cdot d_1 \qquad [2.6]$$

Next, a relationship between E_2 and n_d is developed.

If the donor impurities are assumed to be fully ionized, then the field lines of the ionized charges in the donor layer are terminated by either charge in the channel or charge at the surface. From Gauss' Law, the electric fields emanating from the planar-doping region can be described by:

$$E_2 + E_1 = \frac{qn_d}{\varepsilon_2} \qquad [2.7]$$

which with the help of equation [2.2] may be written as:

$$E_2 = \frac{qn_d}{\varepsilon_2} - \frac{qn_s}{\varepsilon_2} \qquad [2.8]$$

Next substitute equation [2.8] into [2.6] and solve for n_s, and one gets:

$$n_s = \frac{d_2}{d_1 + d_2} \cdot n_d \qquad [2.9a]$$

or equivalently,

$$n_s = \frac{d_2/d_1}{1 + d_2/d_1} \cdot n_d \qquad [2.9b]$$

Equation [2.9] is the called the *Lever Rule*. Clearly, the barrier layer must be larger than the spacer layer in order to transfer the majority of the free carriers in the donor layer to the channel. In the limit as d_2/d_1 is made very large, one obtains:

$$\lim_{d_2/d_1 \to \infty} \frac{n_s}{n_d} = 1 \qquad [2.10]$$

For a high barrier-to-spacer thickness ratio, the model predicts that all the free electrons in the donor layer will transfer to the channel.

2.2 Access Region

There are two design criteria for the access regions of the JHEMT device. First, the access region sheet resistance must be minimized in order to minimize the source and drain parasitic transit delay. Second, the maximum current through the device should not be limited by the available charge in the access region.

Design Philosophy #A1: Minimize Source and Drain Transit Delays

The effects of the source and drain resistance on the total transit delay of the device may be seen by using nodal analysis on a simplified small-signal equivalent circuit model to obtain[4]:

$$\tau_{total} = \tau_{intrinsic} + \tau_{parasitic} \qquad [2.11]$$

$$\tau_{total} = \frac{(C_{gs} + C_{gd})}{g_{mo}} + \frac{(C_{gs} + C_{gd}) \cdot (R_s + R_d)}{g_{mo} \cdot R_{ds}} + C_{gd} \cdot (R_s + R_d) \qquad [2.12]$$

The first term is the intrinsic delay associated with charging the device capacitance. The second two terms correspond to the parasitic time delay through the drain and source resistance, and are particularly important when the gatelength is reduced. The source resistance may be expressed as:

$$R_s = R_{s,access} + R_c = R_{sh,acc} \cdot \left(\frac{L_{gs}}{W_g}\right) + R_c \qquad [2.13]$$

where the first term is the resistance associated with the access region and the second term is the contact transfer resistance which is addressed in Chapter 3. Clearly, a similar expression may be written for the drain resistance. To minimize the parasitic transit delay, the access

sheet resistance ($R_{sh,acc}$) must be minimized. The channel sheet resistance in the access region is given by:

$$R_{sh,acc} = \frac{1}{(q \cdot \mu_e \cdot n_{s,acc})} \qquad \left(\frac{\Omega}{square}\right). \qquad [2.14]$$

Therefore, this design requirement demands both high electron mobility and high electron concentration for minimal sheet resistance in the access region.

Design Philosophy #A2: Maximize the Current Drive Capability

The higher gate barrier of the p$^+$-AlInAs JHEMT allows a higher forward turn-on voltage and, thus, the device may operate in enhancement mode. In such cases, as the gate is biased more positively, additional electrons are induced in the channel (under the gate) and the channel current increases, until one of the following occurs: 1) the gate diode turns on, 2) parasitic MESFET conduction[5] occurs in the AlInAs donor layer, or 3) the electron velocity saturates in the access regions[6] (limiting the available current through the device). The first two points are addressed in section 2.3.3, but, the third point is the focus here. The current (per unit gate width) flowing from the source to the drain is continuous at any point along the channel and may be written as:

$$I = q \cdot n_s(x) \cdot v(x) \qquad (A/cm) \qquad [2.15]$$

where:

q is the electron charge (C)

$n_s(x)$ is the sheet electron concentration (cm^{-2})

$v(x)$ is the electron velocity (cm/s).

The maximum current which may flow through the access region is:

$$I_{max,acc} = q \cdot n_{s,acc} \cdot v_{sat} \qquad (A/cm) \qquad [2.16]$$

which is limited by the maximum number of free carriers ($n_{s,acc}$) in the region, all traveling at the electron saturation velocity (v_{sat}). Even if the gate is able to accumulate many more high velocity electrons, the access regions can not support the additional current. Consequently, the access region resistance rises dramatically[6] causing device figures of merit (e.g. f_T, g_{mo}) to degrade. Therefore, to suppress this phenomena, the access region must be designed for high electron concentration.

2.3 Gate Region

The design of the gate region begins with the derivation of a one-dimensional threshold voltage model which is used to predict threshold voltage. Next, a lumped-element model of the input impedance is discussed which leads to an expression for the gate resistance of the JHEMT. Finally, the design philosophies of the gate region are examined.

2.3.1 Threshold Voltage Model

In this section, a threshold voltage model is derived for the p+-GaInAs/n-AlInAs/GaInAs JHEMT based on the linearized $E_{Fx}(n_s)$ function. Then a modified threshold voltage model is established in order to accurately predict the threshold voltage of the p+-GaInAs/n-AlInAs/GaInAs JHEMTs discussed in Chapter 5.

JHEMT Threshold Voltage Model

The planar-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT is the structure chosen for this calculation. The energy band diagram and electric field of the structure are plotted in Figure 2.3. The following two assumptions are used in the following analysis: i) the donor impurities are fully ionized, and ii) the depletion approximation is valid.

Applying Gauss's Law to the channel, the electric field in the spacer layer may be related to the 2-DEG concentration as:

$$E_1 = \frac{qn_s}{\varepsilon_2} \qquad [2.17]$$

where ε_2 is the dielectric constant in AlInAs. Also from Gauss's Law, the electric field in the barrier layer may related to both the donor sheet density and to the back depletion in the gate layer:

$$E_2 = \frac{qn_d}{\varepsilon_2} - \frac{qn_s}{\varepsilon_2} = \frac{qN_A x_p}{\varepsilon_2} \qquad [2.18a]$$

or more simply,

$$N_A x_p = n_d - n_s \qquad [2.18b]$$

This expression is nothing other than a statement of charge conservation in a closed system with no emerging electric field. Equation [2.18b] may be solved to obtain the back depletion into the gate layer:

$$x_p = \frac{n_d - n_s}{N_A} \qquad [2.19]$$

Next, by solving Poisson's equation under the gate contact, the potentials in the system are related by:

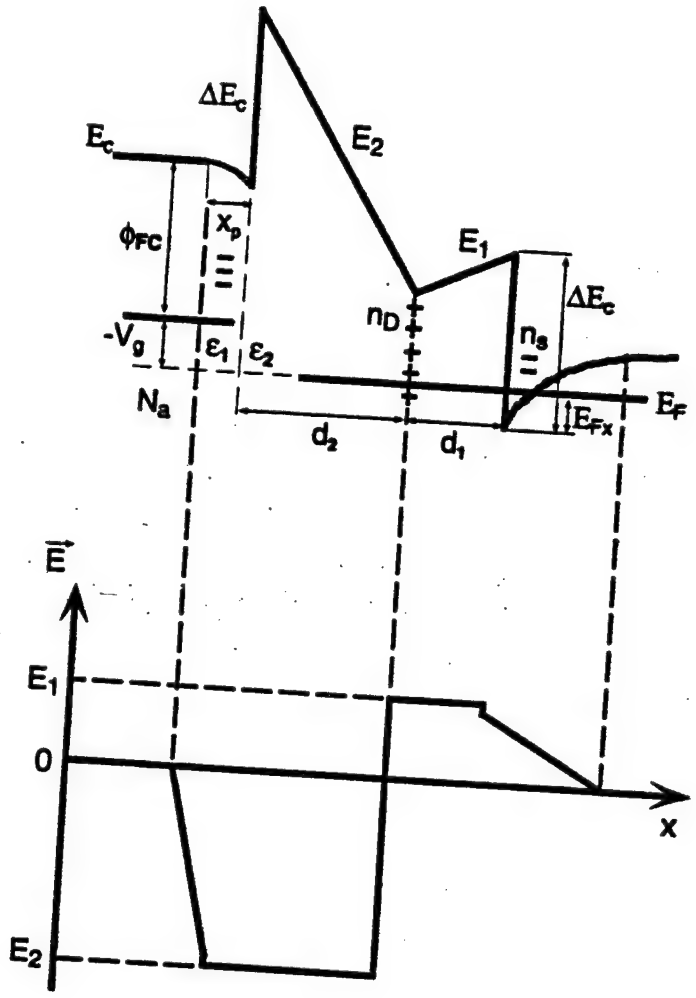


Figure 2.3. Energy band diagram and electric field profile of the planar-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT. The donor layer comprises a sheet of donor atoms, n_d (cm^{-2}).

$$\phi_{FC} - V_g - \frac{qN_a x_p^{\,2}}{2\varepsilon_1} + \frac{\Delta E_C}{q} - \frac{qn_d d_2}{\varepsilon_2} + \frac{qn_s d_2}{\varepsilon_2} + \frac{qn_s d_1}{\varepsilon_2} - \frac{\Delta E_C}{q} + E_{FX} = 0 \qquad [2.20]$$

where ε_1 is the dielectric constant in the GaInAs. Equation [2.20] may be simplified and rewritten by using equations [2.1] and [2.19], and recalling $E_{FO} = 0$ at 300K:

$$\phi_{FC} - V_g - \frac{q(n_d - n_s)^2}{2N_A\varepsilon_1} - \frac{qn_d d_2}{\varepsilon_2} + \frac{qn_s}{\varepsilon_2}(d_2 + d_1) + an_s = 0 \qquad [2.21]$$

By definition, the *threshold voltage* is defined as the gate voltage at which the channel sheet concentration, n_s, approaches zero, or:

$$V_{th} \equiv V_g\Big\|_{\lim_{n_s \to 0}} \qquad [2.22]$$

Applying [2.22] to [2.21] and solving for the threshold voltage, V_{th}, one obtains:

$$V_{th} = \phi_{FC} - \frac{qn_d^{\,2}}{2N_A\varepsilon_1} - \frac{qn_d d_2}{\varepsilon_2} \qquad [2.23]$$

Equation [2.23] is the threshold voltage expression for the planar-doped p$^+$-GaInAs/n-AlInAs/GaInAs JHEMT. In this expression, ϕ_{FC} is the energy from the conduction band to the Fermi level in the gate layer and is limited by the magnitude of the energy bandgap of the p-type semiconductor. For high acceptor concentrations, the second term in [2.23] vanishes and the threshold voltage varies linearly with the thickness of the barrier layer, d_2.

It is often desirable to replace the planar-doped donor layer by a thin, uniformly doped donor region. This allows high electron mobility for very thin spacer layers (see Chapter 5 and see reference[7]). Instead of $n_d\,(cm^{-2})$ electrons in the donor layer, there are now

$N_d \cdot d_n \left(cm^{-2}\right)$ electrons, where d_n is the finite thickness of the uniformly-doped donor layer. The new structure is called the *pseudo-planar-doped (PPD) JHEMT*, and the energy band diagram and electric field are plotted in Figure 2.4. The threshold voltage of the PPD-JHEMT easily derived and given by:

$$V_{th} = \phi_{FC} - \frac{qN_d^2 d_n^2}{2N_A \varepsilon_1} - \frac{qN_d d_n d_2}{\varepsilon_2} - \frac{qN_d d_n^2}{2\varepsilon_2} \qquad [2.24]$$

where the extra (fourth) term is attributed to the potential drop across the uniformly-doped donor region.

Clearly, for extremely high acceptor concentrations where the back depletion into the gate approaches zero ($x_p \rightarrow 0$), one obtains the linear charge control model for Schottky HEMTs (where inherently the depletion in the metal is assumed to be zero). The linear control model first introduced by Delagebeaudeuf and Linh[8] is

$$qn_s = C_s \cdot \left(V_g - V_{th}\right) \qquad [2.25]$$

where C_s is the 2-DEG capacitance per unit area, V_g is the applied gate voltage. Despite the model's simplicity, the linear behavior has been observed in AlGaAs/GaAs HEMTs at 12K[9].

Modified JHEMT Threshold Voltage Model

In the previous threshold voltage model of the planar-doped and pseudo-planar-doped JHEMT, the purpose was to recognize the parameters which heavily influence the threshold voltage. Those model are extremely useful for that reason. However, the linearized $E_{FX}(n_s)$ function (i.e. equation [2.1]) used in those models inaccurately

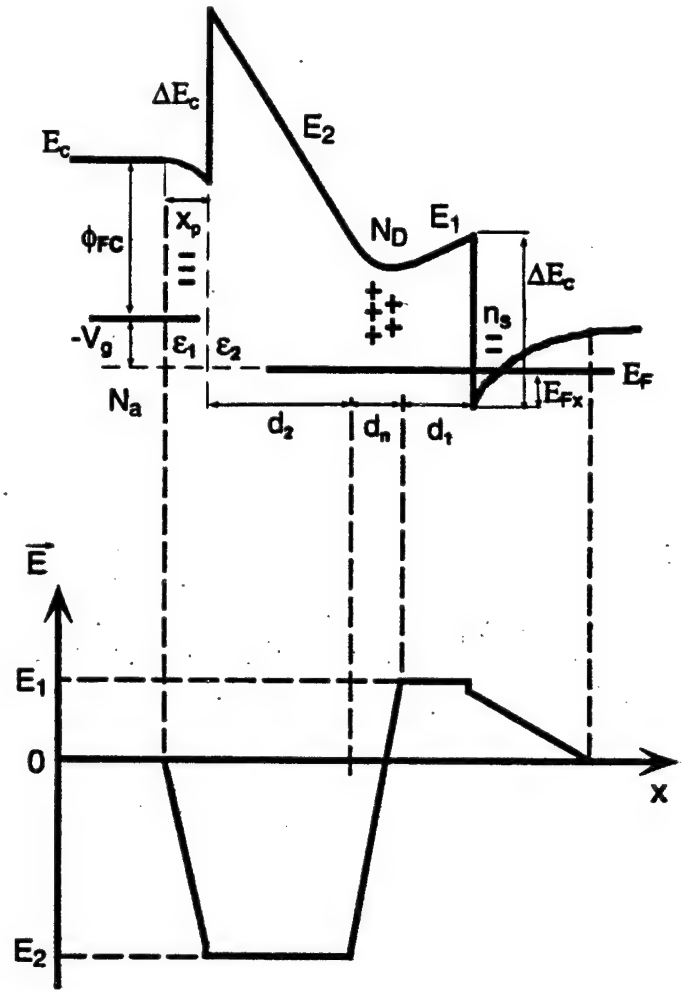


Figure 2.4. Energy band diagram and electric field profile of the pseudo-planar-doped (PPD) p^+-GaInAs/n-AlInAs/GaInAs JHEMT. Instead of a sheet of donor atoms, the donor region consists of N_d (cm^{-3}) over a thickness, d_n.

describes the movement of the Fermi Level as the 2-DEG in the channel vanishes[10]. Therefore, the threshold voltages calculated from the model inaccurately predict the threshold voltage. The purpose here is to derive a relation which accurately describes the threshold voltage in the p+-GaInAs/n-AlInAs/GaInAs pseudo-planar-doped JHEMT.

The analysis begins with recalling the definition of threshold voltage in equation [2.22] and constructing the energy band diagram with a flat-band condition in the channel. The energy band diagram and electric field profile are shown in Figure 2.5. The following assumptions are made in this new model: i) all donor atoms are ionized and their field lines are terminated on acceptor charges in the gate region, ii) at threshold, the channel behaves as if it were intrinsic and the Fermi level has moved near the center of the bandgap (i.e. $E_{F,th} \approx E_g/2$), and iii) the depletion approximation is valid.

Using Gauss's Law, we may write the following charge relation:

$$N_d \cdot d_n = N_A \cdot x_p \qquad [2.26]$$

Again, the back depletion into the gate layer may readily be found when the channel is depleted of free carriers:

$$x_p = \frac{N_d \cdot d_n}{N_A} \qquad [2.27]$$

Now, the potential in the system may be summed to obtain:

$$\phi_{FC} - V_{th} - \frac{qN_A x_p^2}{2\varepsilon_1} + \frac{\Delta E_c}{q} - \frac{qN_A x_p}{\varepsilon_2} \cdot d_2 - \frac{qN_d d_n^2}{2\varepsilon_2} - \frac{\Delta E_c}{q} - E_{F,th} = 0 \qquad [2.28]$$

which after canceling terms and substituting equation [2.27], may be

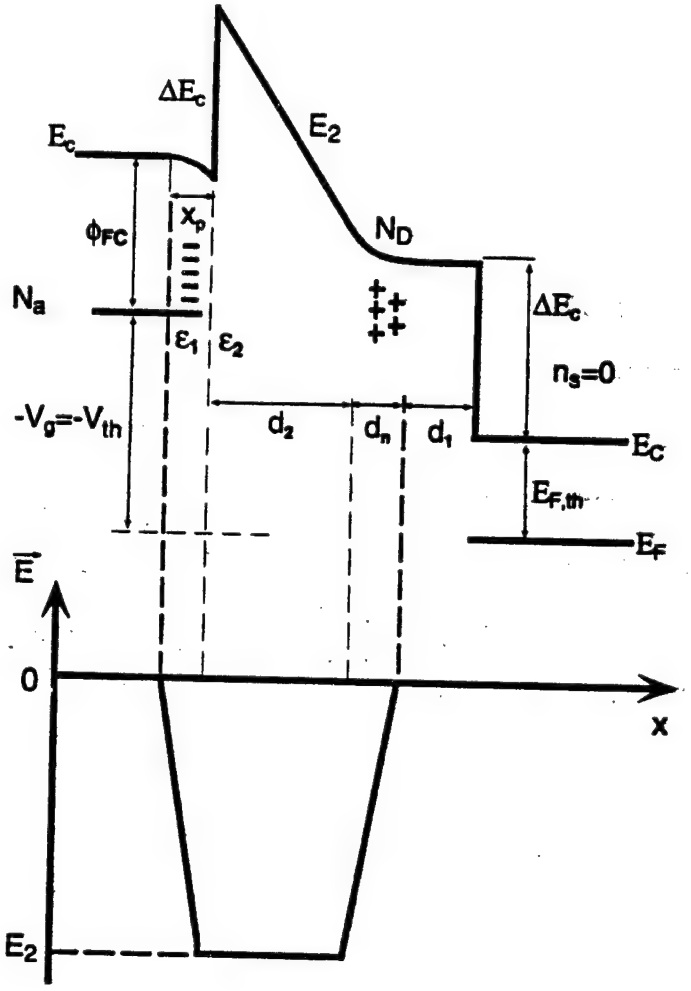


Figure 2.5. Energy band diagram and electric field profile of the pseudo-planar-doped (PPD) p^+-GaInAs/n-AlInAs/GaInAs JHEMT at the threshold condition. Solving the electrostatics with the position of the Fermi Level near the middle of the energy gap leads to the accurate calculation of the threshold voltage.

simplified to get:

$$\phi_{FC} - V_{th} - \frac{qN_d{}^2 d_n{}^2}{2N_A\varepsilon_1} - \frac{qN_d d_n}{\varepsilon_2}\cdot d_2 - \frac{qN_d d_n{}^2}{2\varepsilon_2} - E_{F,th} = 0 \qquad [2.29]$$

Solving for the threshold voltage, one gets

$$V_{th} = \phi_{FC} - \frac{qN_d{}^2 d_n{}^2}{2N_A\varepsilon_1} - \frac{qN_d d_n}{\varepsilon_2}\cdot d_2 - \frac{qN_d d_n{}^2}{2\varepsilon_2} - E_{F,th} \qquad [2.30]$$

Equation [2.30] is the modified threshold voltage equation for the pseudo-planar-doped JHEMT. As an example, the threshold voltage of wafer #V1307C (reported in Chapter 5) is estimated using the original charge control model and also calculated using the modified (flat-band condition) model. The results are listed in the table in Figure 2.6. The modified model developed here more accurately predicts the threshold voltage. The difference between the two models is accounted for by the relative position of the Fermi Level when the threshold condition is satisfied. In this case, the difference in the two models is $E_g/2$=0.375eV.

Wafer V1307C		V_{th}
Measure	50 Devices	-.76 to -.81V
Model	Charge Control Threshold Voltage Model	-0.34V
Model	Flat-Band Threshold Voltage Model	-0.71V

Figure 2.6. Threshold voltage model comparison with actual devices measure on wafer V1307C. The Flat-Band Model (derived from Figure 2.7) more accurately predicts the threshold voltage due to the corrected assumptions about the position of the Fermi Level.

2.3.2 *JHEMT Input Impedance Model*

The use of a junction to modulate the 2-DEG introduces an extra gate resistance, in addition to the gate metal resistance, corresponding to the contact resistance of the gate metal electrode to the p-type gate region. The purpose of this section is to develop a simple expression to describe the input impedance of the JHEMT.

Since the input signal applied from the feeding end of the gate propagates along the gate metallization to the other end, the gate has to be analyzed as a distributed network. Wolf[11] developed the lumped-element model of the distributed network used for the Schottky-gate HEMT. However, this model does not account for contact resistivity from the metal to the semiconductor. Thus, the analysis of Wolf is expanded to include the additional gate resistance in the JHEMT.

The gate finger of the JHEMT is treated as an open-circuit transmission line. The unit cell of the transmission line consists of a single series impedance along with a shunt-admittance. The input impedance of the transmission line is then approximated by a power series expansion and a lumped-element approximation of the JHEMT input impedance is obtained. The cross-section, unit cell, and lumped element impedance model of both the HEMT and JHEMT is given in Figure 2.7. The full mathematical derivation of the lumped element impedance model is given in Appendix A. Consistent with Wolf's analysis (applied to the Schottky HEMT), the same reduced value of metallization resistance (one-third of the end-to-end dc resistance)

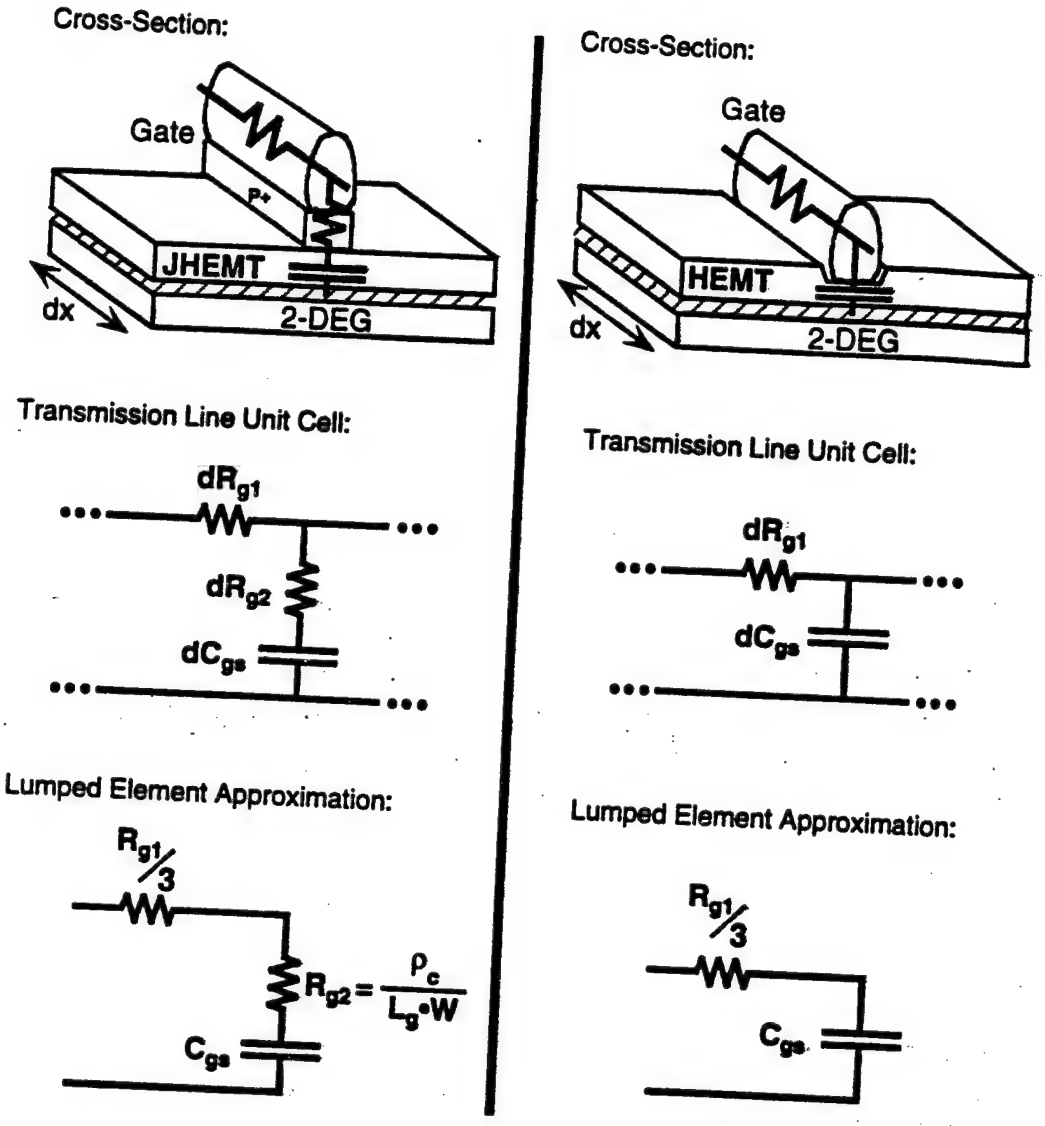


Figure 2.7. Summary of the lumped-element model for both the JHEMT (Left) and the HEMT (right). The infinitesimal cross-section of gate width, dx (top), the unit cell of the transmission line used to model the gate finger (middle), and the lumped-element approximation of the gate input impedance (bottom) are compared.

and the total gate capacitance is obtained. However, an additional series resistance associated with the ohmic contact to the p-type region (R_{g2}) is present in the JHEMT lumped-element model. The magnitude of this resistance is proportional to the specific contact resistivity (in Ω-cm^2) of the gate metal to the p$^+$-region and inversely proportional to the gate length. The scalability issues which arise due to the presence of this second gate resistance are addressed in the next section.

Finally, the total gate resistance including the metal feed resistance may be written as:

$$R_g = R_{g,feed} + \left(\frac{R_{gee}}{W}\right)\cdot\frac{W}{3n^2} + \frac{\rho_c}{L_g \cdot W} \qquad [2.31]$$

Experimentally, the feed resistance accounts for at least 10 percent[12] of the total resistance and is not negligible.

2.3.3 Gate Layer Design

In past years, the junction barrier gate has not been the leading gate technology for III-V FETs due to: (i) the additional gate resistance associated with the ohmic contact to the p-type region, and (ii) the hole injection from the gate into the channel. Further, back depletion into the gate layer effectively increases the gate-to-channel separation. These three issues are addressed in the following five design philosophies.

Design Philosophy #G1: Low Gate Contact Resistivity

The gate metal-semiconductor contact should have a low contact resistivity. As discussed in the previous section, the additional gate

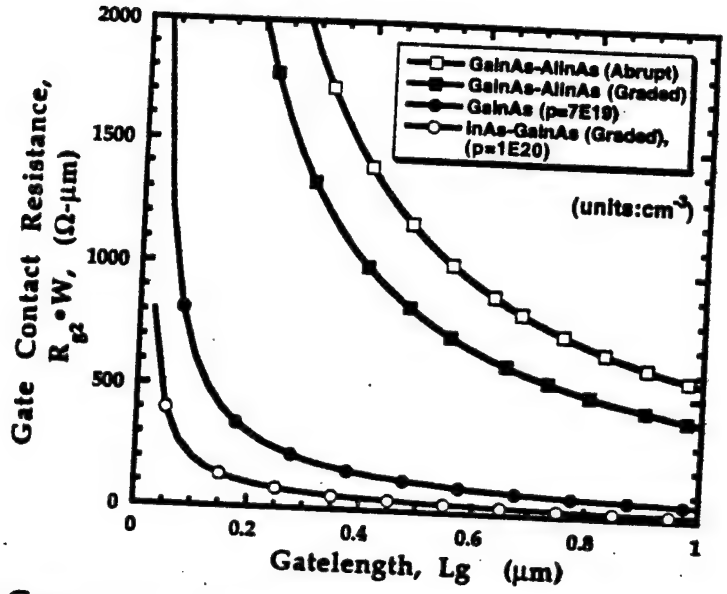


Figure 2.8 Gate contact resistance, R_{g2} , versus gatelength for various gate materials. Notice the high resistance for gate regions containing AlInAs. The ohmic contacts are non-alloyed *Ti / Pt / Au* metal contacts. (The contact resistivity values used here were taken from a study by P. Chavarkar and M. Mondry, unpublished).

resistance, R_{g2}, in the JHEMT is given by:

$$R_{g2} = \frac{\rho_c}{L_g \cdot W_g} \qquad [2.32]$$

Therefore, as the gatelength of the JHEMT is reduced, the gate contact resistivity becomes increasing more crucial. A plot of gate contact resistance (in Ω-μm) versus gatelength for various gate materials is shown in Figure 2.8. This plot makes three important points regarding the design of the gate region of the JHEMT. First, at long gatelengths the contact area of the gate is high, making the gate contact resistance in

equation [2.31] small even for materials with higher contact resistivity. Second, at short gatelength such as 0.2μm, the contact area of the gate is small, making the material selection of the gate material crucial to maintaining low gate contact resistance. Third, there is a distinct trade-off between having a high gate barrier and having a small gate contact resistance (R_{g2}), especially at short very gatelengths. Therefore, for example, it is quite difficult to design an enhancement-mode, 0.1μm gatelength JHEMT which operates at a forward gate voltage of 1V and requires low gate resistance.

Design Philosophy #G2: Optimize Gatewidth

Further, the optimal gatewidth may be found by minimizing the expression for extrinsic gate resistance shown in equation [2.31]. Differentiating with respect to gatewidth leads to:

$$\frac{\partial R}{\partial W} = \left(\frac{R_{gee}}{W}\right) \cdot \frac{1}{3 \cdot n^2} - \frac{\rho_c}{L_g \cdot W^2} = 0 \qquad [2.33]$$

which can be solved for optimum gatewidth:

$$W_{opt} = \sqrt{\frac{3n^2 \rho_c}{\left(R_{see}/W\right) \cdot L_g}} \qquad [2.34]$$

For the 0.2μm gatelength, p+-GaInAs gate JHEMT ($\rho_c = 3x10^{-7} \Omega \cdot cm^2$, $R_{see}/W = 250\Omega/mm$, n=2 fingers), the optimum gatewidth is 85μm. For the 0.2μm gatelength, graded p+-GaInAs/p+-AlInAs gate JHEMT ($\rho_c = 5x10^{-6} \Omega \cdot cm^2$, $R_{see}/W = 250\Omega/mm$, n=2 fingers), the optimum gatewidth is 345μm. The gatewidths chosen for the p+-GaInAs gate and the p+-GaInAs/p+-AlInAs gate JHEMT were 100μm and 300μm,

respectfully. The expression for optimum gatewidth does not include the effects such as cross-over capacitance in cases where n>2 fingers. Therefore, equation [2.34] applies to cases where n≤2 fingers.

Design Philosophy #G3: Low Hole Injection

Hole injection into the channel is undesirable. This can be prevented by introducing a large barrier for holes (most conveniently in the form of ΔE_v). Similar to a npn-HBT, the JHEMT requires a large ratio of electron current (from the channel to the gate) to hole current (from the gate to channel).

Design Philosophy #G4: High Acceptor Doping in the Gate Region

The gate region should be doped as heavily as possible to: i) minimize the back depletion in the gate layer, ii) achieve the lowest contact resistivity to the gate region, and iii) provide the largest gate potential possible.

Recall from equation [2.19] that the back depletion is given by:

$$x_p = \frac{n_d - n_i}{N_A} \qquad [2.35]$$

Thus, for a high acceptor doping in the gate region, the back depletion is minimized. Properly minimizing the back depletion results in a reduced gate-to-channel separation which increases the intrinsic gate capacitance. Increasing the acceptor concentration also results in lower contact resistivity. For p^+-GaInAs ($p=1\times10^{20}cm^{-3}$), the contact resistivity achieved is $3\times10^{-7}\Omega\text{-}cm^2$ which (from Figure 2.8) is suitable for short gatelengths (e.g. 0.2μm). Finally, the electron built-in potential of the

diode increases with increasing acceptor doping up to a maximum, which is the energy bandgap of the gate material.

Design Philosophy #G5: High-Aspect-Ratio/Fully Ionized Donor Layer

There are two requirements of the modulation-doped layers under the gate layer. First, the gate-to-channel separation must be scaled proportionately with the gatelength so an aspect-ratio[13] ($L_g/d_{gate-2DEG}$) of at least 6 is maintained. This provides a high voltage gain (g_m/g_o) and a high capacitance ratio (C_{gs}/C_{gd}), which assures high power gain. Second, the thickness and doping of the donor layer are such that all the electrons in the donor layer are depleted at equilibrium and remain depleted under any desirable bias condition (e.g. forward gate-voltages). This ensures that parasitic MESFET conduction will not occur[5].

References

[1] The Lever Rule is reproduced here for easy reference. The importance of the layer thicknesses is discussed in earlier work by: K. Lee, M. Shur, T. Drummond, and H. Morkoc, "Electron Density in the Two-Dimensional Electron Gas Modulation-Doped Layers," J. Appl. Phys., Vol. 54, No. 4, pp. 2093-2096, 1983.

[2] K. Lee, M.S. Shur, T.J. Drummond, and H. Morkoc, "Current-Voltage and Capacitance-Voltage Characteristics of Modulation-Doped Field-Effect Transistors," IEEE Trans Electron Dev., Vol. ED-30, pp. 207-212, Mar. 1983.

[3] This linearized expression is only an approximation which is well fitted up to $1.5x10^{12}cm^{-2}$. The type of numbers we are typically designing for are $2\text{-}3x10^{12}cm^{-2}$. The validity of this expression for our 2-DEG concentrations is questionable and for more exact calculations, such as the I-V calculations in Chapter 4, this approximation is not used. However, the purpose of this model is to understand the charge distribution in the device and this expression for a simple,complete analysis. It also may be argued that this expression is not key to the arguments made in the model.

[4] P.J. Tasker and B. Hughes, "Importance of Source and Drain Resistance to the Maximum f_t of millimeter-wave MODFETs," IEEE Electron Dev. Lett., Vol. 10, July 1989.

[5] K. Lee, M.S. Shur, T.J. Drummond, and H. Morkoc, "Parasitic MESFET in (Al, Ga) As/GaAs Modulation Doped FETs and MODFET Charcterization," IEEE Trans Electron Dev., Vol . ED-31, pp. 29-35, Jan 1984.

[6] D.R. Greenberg, and J.A. del Alamo, "Velocity Saturation in the Extrinsic Device: A Fundamental Limit in HFETs," IEEE Trans. on Eletron Dev., Vol. 41, No. 8, August 1994.

[7] L.D. Nguyen, A.S. Brown, M.A. Thompson, L.M. Jelloian, "50-nm self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors", IEEE Trans. Electron Dev., Vol. 39, pp. 2007-2014, 1992.

[8] D. Delagebeaudeuf and N.T. Linh, "Metal-(n)AlGaAs-GaAs Two-Dimensional Electron Gas FET," IEEE Trans. Electron Dev., Vol. ED-29, pp. 955-960, June 1982.

[9] K. Hirakawa, H. Sasaki, and J. Yoshino, "Concentration of Electrons in Selectively-Doped GaAlAs/GaAs Heterojunctions and its Dependence on Spacer Layer Thickness," Apply. Phys. Lett., Vol. 45, No. 3, pp. 253-255., Aug. 1, 1994.

[10] The Linearizd Fermi Function predicts that the Fermi Level is coincident with the conduction band when the 2-DEG approaches zero. The authers who suggested reported equation 2.1 stated that the expression was only valid from $n_s = 8x10^{11}$ to $1.5x10^{12}cm^{-2}$.

[11] P. Wolf, "Microwave properties of Schottky Barrier FETs", IBM J. Res. Develop., Vol .14, pp. 125-141, March 1970.

[12] This value is based upon the 100μm wide, single feed JHEMTs discussed in Chapter 5.

[13] M.B. Das, "A High Aspect Ratio Design Approach to Millimeter-Wave HEMT Structures,", IEEE Trans. on Electron Dev. , Vol. ED-32, No. 1, Jan. 1985.

Chapter 3
JHEMT Process Technology and Material Characterization

The key to achieving uniformity in the gate region of the JHEMT is the preservation of the gate-to-channel separation. To this end, the fabrication process is designed such that the gate variations observed across a wafer are exclusively due to non-uniformities in the MBE growth. In this chapter, the fabrication process is described for the mm-Wave JHEMT including the regrowth process. This is followed by a summary of the two ohmic contact technologies utilized in this work to fabricate JHEMTs. Finally, the procedure used to characterize the JHEMT epitaxial structure is discussed.

3.1 Fabrication Process

The fabrication procedure of the JHEMT is influenced most heavily by the ohmic contact technology and the gate technology utilized. The source and drain contact may either be regrown or alloyed to achieve electrical contact to the 2-DEG of the JHEMT. The gate contact chosen may comprise either a refractory metal or a non-refractory metal (e.g. transition metal, noble metals), and may have been formed using either optical lithography or e-beam lithography. These technological choices ultimately determine the fabrication procedure. This section focuses on the regrowth procedure, then discusses the JHEMT process using a non-refractory gate metal.

3.1.1 Regrowth of Ohmic Contacts by MOCVD

Growth of the lattice matched n-InGaAs contact layer was achieved by low pressure metal-organic chemical vapor deposition (MOCVD). (The MOCVD regrowth was accomplished by *Majid Hashemi* and *Mark Heimbuch* of UCSB.) The sources were trimethylindium (TMI), trimethylgallium (TMG), tertiarybutylarsine (TBA) and disilane (150ppm in hydrogen) for the n-type source[1]. The liquid organometallic group V source, TBA was purchased from Air Products and Chemicals, Inc. Bubbler temperatures were kept at 5°C, -10°C and 20°C for the TBA, TMGa, and TMIn sources, respectively. To eliminate organometallic vapor condensation all the source lines are resistively heated from the output of the bubblers to the injection manifold. The reactor employs two separate injection manifolds to keep group-V and group-III sources separate until they are mixed immediately upstream from the susceptor. This design was implemented to avoid any adduct formations that might occur between the group-III alkyls and the organometallic group-V sources.

Before regrowing the contact layers, the bulk InGaAs doping characteristics with TBA and disilane were optimized[2]. A 150 ppm disilane in hydrogen mixture is used for n-doping of InGaAs. Linear doping behavior is observed for both InP and $In_{0.53}Ga_{0.47}As$ epilayers over a wide range of conditions. For completeness, Appendix B shows a plot of flow-rate of the disilane/hydrogen mixture versus carrier concentration at room temperature. A relatively high n-doping saturation of $5x10^{19}cm^{-3}$ in the InP is achieved when using TBP. For the n-InGaAs

regrown contact layer a doping level of $2x10^{18}$ cm^{-3} was employed. The best undoped $In_{0.53}Ga_{0.47}As$ epilayers had 77K mobilities of 59,000$cm^2/V{\cdot}s$ and unintentional background impurity level of $5.5x10^{15}$ cm^{-3}.

At a growth temperature of 600°C and reactor pressure of 100 Torr, good selectivity was achieved and no deposition was observed on the oxide mask. The sample was initially heated up to 650°C for 3 minutes to remove the native oxide layer and produce specular morphology regrowth. Complete selectivity of the regrown InGaAs was obtained because of the increased diffusivity of the column III species at 100 Torr. The growth rate for regrown InGaAs epilayers in the device structure was approximately 11Å/sec. A V/III ratio of 22 ensures specular surface morphology at 100 Torr. A total gas flow rate of 5.5 slpm was found to yield a uniform film deposition in our system.

The complete regrowth process is summarized in the flow diagram given in Figure 3.1. First, SiO_x (typically, 1000Å) is deposited using an ECR Plasma-Therm™ oxide/nitride system. Using optical lithography and the ohmic level mask, the source and drain windows are opened in the 1μm-thick AZ P5214 resist. Next, the exposed oxide is etched back to the wafer surface using CF_4 plasma (100W/300mT). The oxide etch-rate varied, but was typically 150-200Å/minute. Once the oxide was believed to be removed, the sample was dipped into concentrated Buffered Hydrofluoric Acid (BHF or BOE[3]) for 5 seconds to ensure complete removal. Then, the gate layer(s), barrier layer, donor layer, spacer layer,

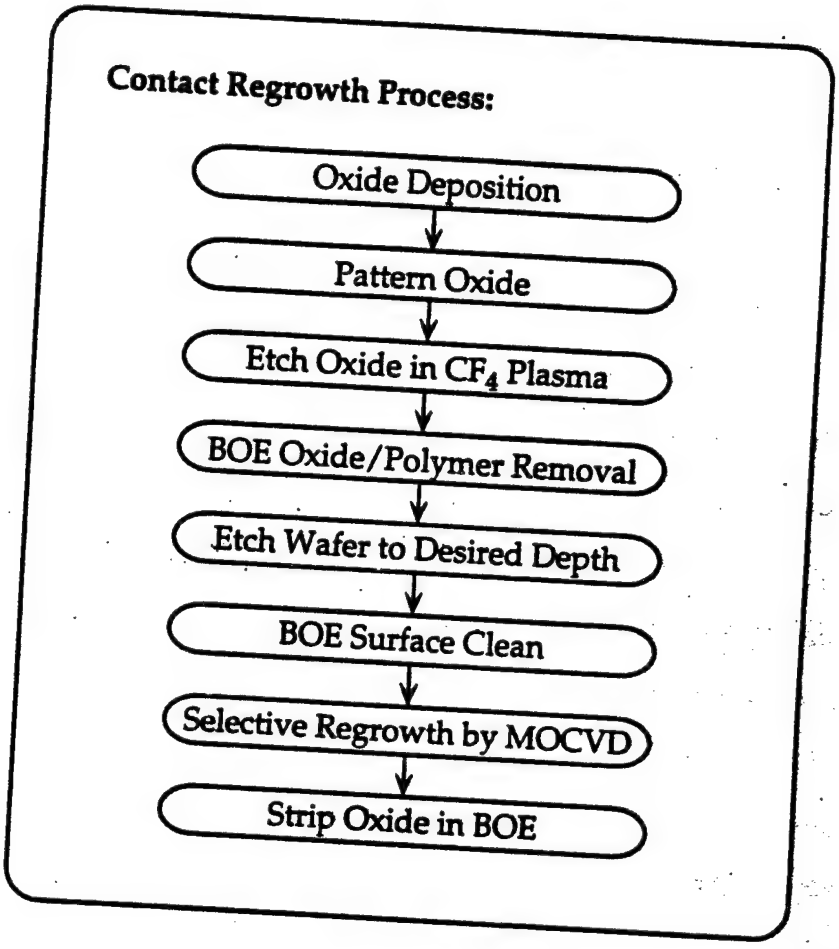


Figure 3.1. Flow diagram representing the ohmic contact regrowth process.

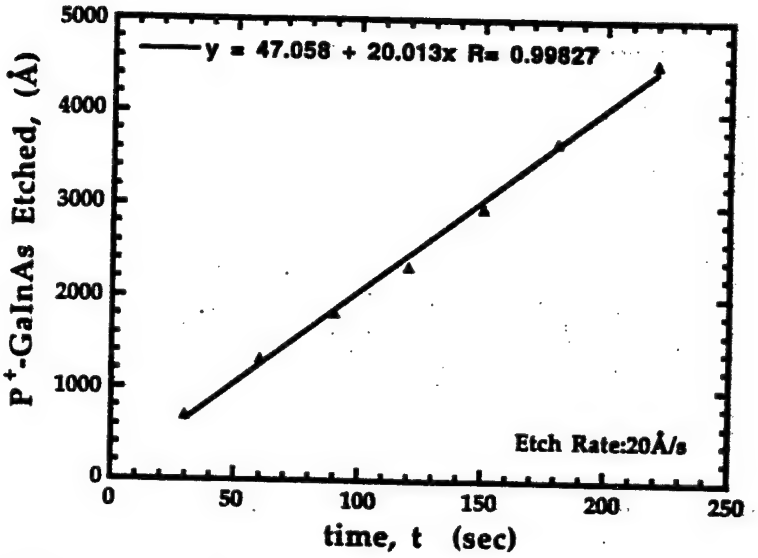


Figure 3.2. Etch rate calibration of the phosphoric acid solution used during the ohmic region etch. From the slope of the line, the etch rate of the H_3PO_4:H_2O_2:H_2O solution is 20Å/s. The material used for the calibration is GaInAs:Be ($p=5x10^{18}$ cm^{-3}).

and the top 100Å of the channel were removed using a stirred-solution of $H_3PO_4:H_2O_2:H_20$ (3:1:50). The GaInAs etch rate of this solution, from Figure 3.2, is 1200Å/min when stirred at 200RPM. Before loading the sample into the reactor, the sample was dipped in BOE for 5 seconds, rinsed for 2 minutes in de-ionized water, and blown dry with N_2. The ohmic regions were regrown with the top of the regrowth targeted at 500Å above the wafer surface. After regrowth, the sample was etched in concentrated BOE to remove the SiO_x mask.

3.1.2 mm-Wave JHEMT Fabrication Process

As mentioned in Chapter 1, the principal difference between the fabrication of the JHEMT and the HEMT is the gate recess etch . In the HEMT the recess etch precedes the deposition of the gate metal. By comparison, the recess (or access region) etch in the JHEMT occurs after the gate metallization. The isolation (mesa) etch occurs after the gate is deposited in order to prevent gate leakage along the mesa sidewall[4]. The order in which the ohmic metal is deposited is not critically dependent on the other steps[5]. However, if the ohmic contacts require a high temperature anneal, then the gate metal must be able to withstand the temperature treatment.

In the mm-Wave JHEMT, *Ti / Pt / Au* is selected as the gate metal for two reasons. First, *Ti / Pt / Au* is compatible with the existing bi-layer resist technology used to form the T-shaped gate. Second, low contact resistivity to p^+-GaInAs are achieved using *Ti / Pt / Au* as shown in Figure 2.10. However, it is observed that TiPtAu gate metal penetrates through

the gate region at a temperature of 330-340°C. Since the ohmic contact alloy temperature is typically 350-355°C, the gate must be deposited after the ohmic contacts are alloyed. The cross-sections given in Figure 3.3 summarize the main process steps used to fabricate the mm-Wave, p^+-GaInAs/n-AlInAs/GaInAs JHEMT.

Source/Drain Metal Contacts

First, the source and drain contacts are deposited (*Ni*(100Å) / *AuGe*(900Å) / *Au*(2000Å)) in an e-beam metal evaporator. The surface oxide is removed by dipping the sample in BOE for 5 seconds and rinsed for 2 minutes prior to loading the sample in the evaporator. Then, these metal contacts are directly deposited on the p^+-GaInAs gate region. The deposition of the contacts on top of the p-region rather than recessing them into the p-region is the topic of discussion in section 3.2.2.

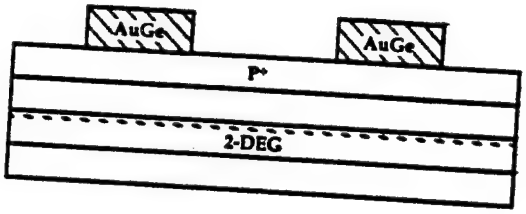
Implant Isolation

The wafer is selectively implanted with Boron atoms to isolate both the active devices and the test structures (e.g. TLM patterns). (The implant was accomplished by *Bob Wilson* of Hughes Research Laboratories). Isolation at this stage enables step-by-step monitoring of device parameters such as contact transfer resistance, sheet resistance, and current density throughout the rest of the process. The dose and energy of each implant (as shown in Figure 3.3) were selected to obtain a desired range and straggle of Boron impurities.

Anneal

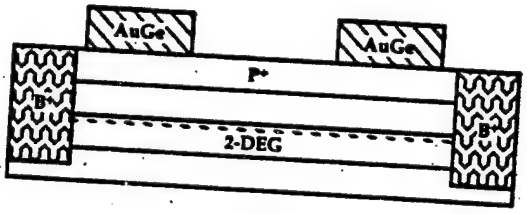
The source and drain metal contacts are alloyed through the gate

Step 1: Source/Drain Metallization:
Ni/AuGe/Au, 100Å/900Å/2000Å



Step 2: Implant Isolation (Boron):

1) 100kV, $2x10^{12}$ cm^{-2}
2) 50kV, $1x10^{13}$ cm^{-2}
3) 20kV, $2x10^{13}$ cm^{-2}
4) 10kV, $5x10^{13}$ cm^{-2}



Step 3: Ohmic Contact Anneal:
355° C, 50 seconds.

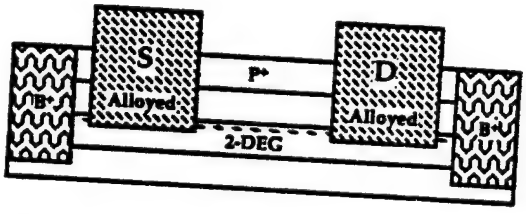
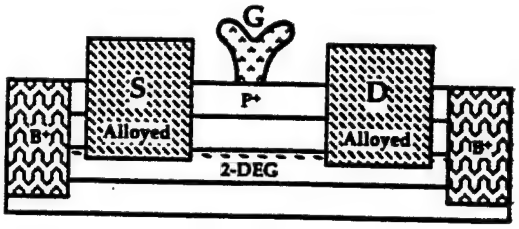
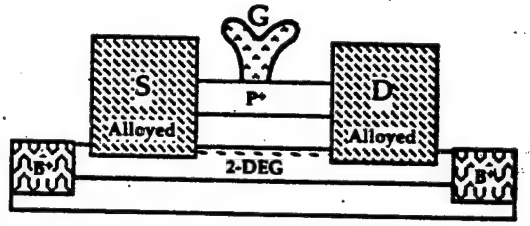


Figure 3.3. Summary of the process steps used to fabricate the p+-GaInAs/n-AlInAs/GaInAs JHEMT.

Step 4: Sub-micron, T-Shaped Gate Formation:
Bi-Level Resist Process
Ti/Pt/Au/Ni, 500Å/500Å/3000Å/1000Å.



Step 5: Mesa/Gate Pad Isolation:
H_3PO_4:H_2O_2:H_2O, 3:1:50.



Step 6: Gate Recess (Access Region) Etch:
H_3PO_4:$C_6H_8O_7$:H_2O_2:H_2O, 1:100:10:400.

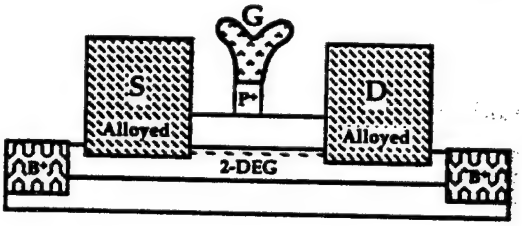


Figure 3.3. (continued)

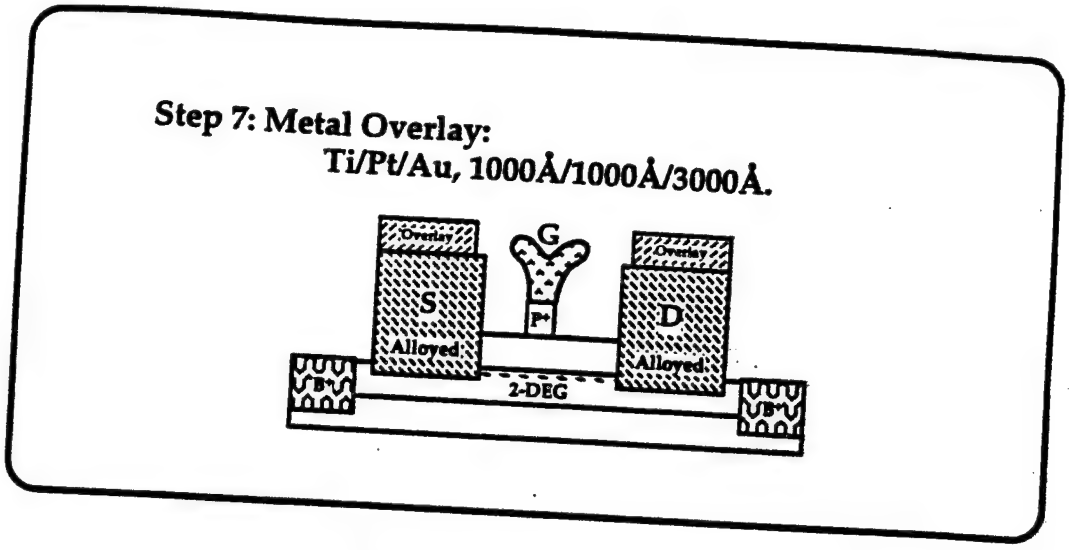


Figure 3.3. (continued)

region into the channel at a temperature which is previously determined to be the optimal alloy temperature. The optimum condition was determined to be 355° for 50 seconds. Section 3.2 discusses the TLM measurements which were used to determine the optimum anneal temperature. In addition, the alloyed ohmic contact technology and regrown n^+-GaInAs (non-alloyed) ohmic contact technology are also compared.

Sub-Micron Gate Formation

Two different 0.2μm gate length structures were studied in this work: i) a triangular-shaped gate, and ii) a mushroom or T-shaped gate. (The e-beam gates were written, developed, and inspected by *Mark Thompson* of Hughes Research Laboratories.) The T-shaped gate is utilized to reduce the metal end-to-end resistance which determines the gate metal

resistance according to equation [A.9] (See Appendix A). In Figure 3.4, the metal end-to-end resistance of each gate geometry is given. Clearly, by utilizing a T-shaped gate, the metal gate resistance of a 0.2μm gate JHEMT (or HEMT) may be reduced by more than a factor of 3. The T-shaped gate is defined using a bi-level resist process. The gate metal is $(Ti(500\text{Å}) / Pt(500\text{Å}) / Au(3000\text{Å}) / Ni(1000\text{Å}))$, where the Ni cap on the gate metal is included to protect the Au in cases where the mesa is dry-etched in a Cl_2 R.I.E.

Gate Geometry	$\frac{R_m}{W}$ Ω/mm
Triangular-shaped	820
T-shaped	250

Figure 3.4. The metal end-to-end resistance of the 0.2μm gate with different geometry's.

Isolation Mesa

Then, the isolation mesa is defined using a stirred solution of $H_3PO_4:H_2O_2:H_20$ (3:1:50). This isolation mesa etch in the JHEMT has two purposes. First, the mesa isolates the active region, similar to the Schottky-gate HEMT process. Second, this etch also undercuts the gate feed into the active region. Undercutting the gate feed effectively isolates the gate pad from the intrinsic device. Further, if the isolation mesa is defined using a Cl_2 R.I.E., then the dry etch must be followed by a wet

etch in order to isolate the gate pad.

Gate Recess Etch

Afterwards, the access regions are defined using a settled, citric acid-based solution of H_3PO_4:$C_6H_8O_7$:H_2O_2:H_20 (1:100:10:400). The citric acid was purchased from VWR Chemical Supply. The data (from an etch experiment) used to determine the etch rate of the solution is given in Figure 3.5. The purpose of the gate recess etch is two-fold. First, the electrical gatelength is determined when the gate footprint is defined. This differs from the Schottky-gate HEMT, where the metal footprint determines the electrical gatelength. Second, the surface potential drops when the p^+ surface layers are removed, reducing the channel sheet resistance in the access regions. The variation of the sheet resistance with this recess etch is the main topic addressed in section 3.3.

Overlay Metal

Finally, the overlay metal ($Ti(1000\text{Å}) / Pt(1000\text{Å}) / Au(3000\text{Å})$) is deposited in order to provide a good thick contact layer for all subsequent measurements. This thick layer provides extra cushion for the microwave probes and prevents the probes from being damaged when the devices are tested.

The interested reader is directed to Appendix C where the JHEMT process traveler is given detailing each of the main steps discussed here.

3.2 Ohmic Contact Technology: Contact Transfer Resistance

The purpose of this section is to compare and summarize the

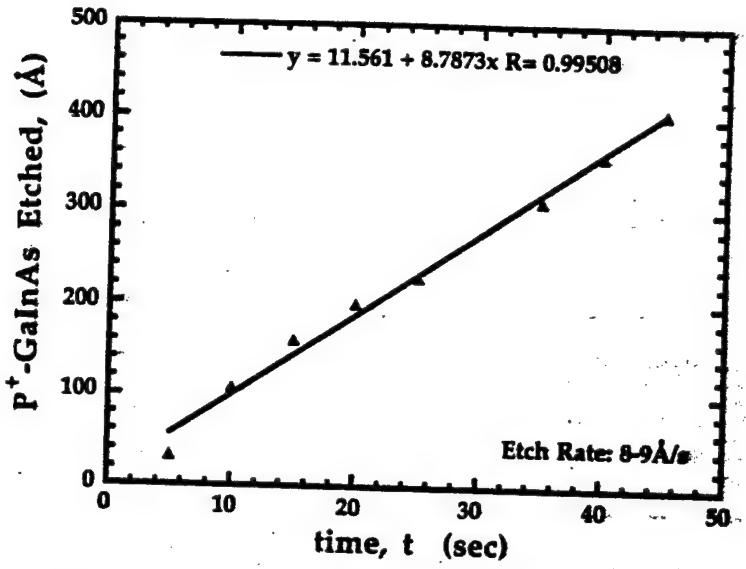


Figure 3.5. Etch rate calibration of the citric acid based solution used during the recess (or access region) etch. From the slope of the line, the etch rate of the H_3PO_4:$C_6H_8O_7$:H_2O_2:H_2O solution is 8-9Å/s. The material used for the calibration is GaInAs:Be ($p=3x10^{19}$ cm^{-3}).

results of the two ohmic contact technologies studied in this work, specifically: i) non-alloyed regrown ohmic contacts, and ii) alloyed AuGe ohmic contacts. Both contact technologies were studied on 1μm and 0.2μm gatelength JHEMTs.

3.2.1 Regrown Ohmic Contacts

Non-alloyed regrown (n^+-GaInAs) ohmic contacts were studied on two single-modulation-doped wafers. The regrown regions of both wafers start approximately 100Å into the channel as discussed in section

3.1.1. The contact transfer resistance of the two wafers is summarized in Figure 3.6. The contact transfer resistance of the wafers was 0.45 and 0.5 Ω-mm. For the 0.2μm gatelength JHEMT, if the contact transfer resistance is 0.5 Ω-mm, then the majority of the total transit delay will be parasitic delay (dominated by high source and drain resistance) as describe by equation [2.16]. Clearly, the contact transfer resistance must be reduced in order for this technology to be useful for sub-micron gatelength devices.

Wafer #	Modulation-Doped Channel Structure	Contact Transfer Resistance
V646A	Single-Doped 300Å GaInAs	0.45 Ω-mm
930920C	Single-Doped 300Å GaInAs	0.5 Ω-mm

Figure 3.6. Contact resistivity obtain in single-doped channel structures using regrown n^+-GaInAs contact regions.

3.2.2 Alloyed Ohmic Contacts

Alloyed ohmic contacts were extensively studied on the p^+-GaInAs/n-AlInAs/GaInAs JHEMT structure. The thickness of the p^+-GaInAs gate region ($p=1x10^{20}cm^{-3}$) was 200Å. The effectiveness of recessing the metal contacts into the p^+-GaInAs was studied using two samples. The control wafer consisted of TLM structures fabricated (i.e. both metallization and isolation process steps) without recessing the contacts, simply placing them on the 200Å-thick, p^+-GaInAs. The test wafer consisted of TLM structures fabricated by recessing the contacts 150Å into the 200Å-thick gate region. On both samples, the contacts were

alloyed under various condition to determined the minimum contact transfer resistance obtainable.

The highlights of the TLM experiments are given in Figure 3.7. TLM data at 350°C for both samples with and without recessed contacts are shown in the top of the figure. The data indicates that similar contact transfer resistance may be obtained whether the ohmic contacts are recessed into the p-region or not. Further, in the bottom of the figure, the contact transfer resistance is plotted versus alloy temperature. At 350°C, the contact transfer resistance of the two samples is very similar. But at temperatures below 350°C, the contact transfer resistance is lower for the test sample compared to the control sample. This is attributed to the fact that the non-recessed contact must, first, alloy through the p^+-region before low contact transfer resistance to the channel is obtained.

Technologically speaking, the non-recessed ohmic contact is more advantageous for the JHEMT structure. First, no precise recess etching of the metal contacts is required, thus reducing the complexity of the fabrication process. Second, eliminating the contact recess etch eliminates the trenching at the source and drain contact edge during the gate recess etch. The trenching occurs because the lift-off mask is undercut during the contact recess etch. Once, the undercut exists, the gate recess etch removes more of this undercut region causing a trench in the final device profile. The trench is evident in the cross section shown in Figure 3.8. This trenching effectively increases the source and drain resistance, increasing the total transit-delay through the device.

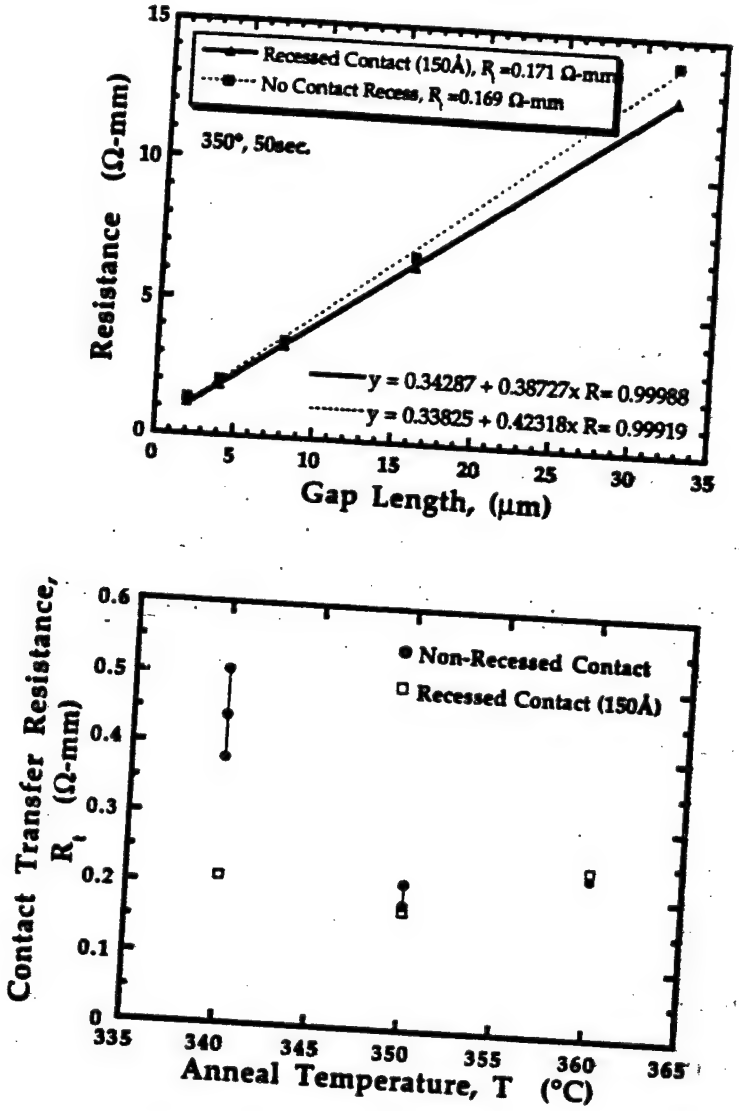


Figure 3.7. TLM data for recessed ohmic contacts (150Å) and non-recessed ohmic contacts for the p$^+$-GaInAs/n-AlInAs/GaInAs JHEMT. The contact transfer resistance of the samples is similar at 350°C (top). The contact transfer resistance of the recessed contact is lower at temperatures below 350°C (bottom).

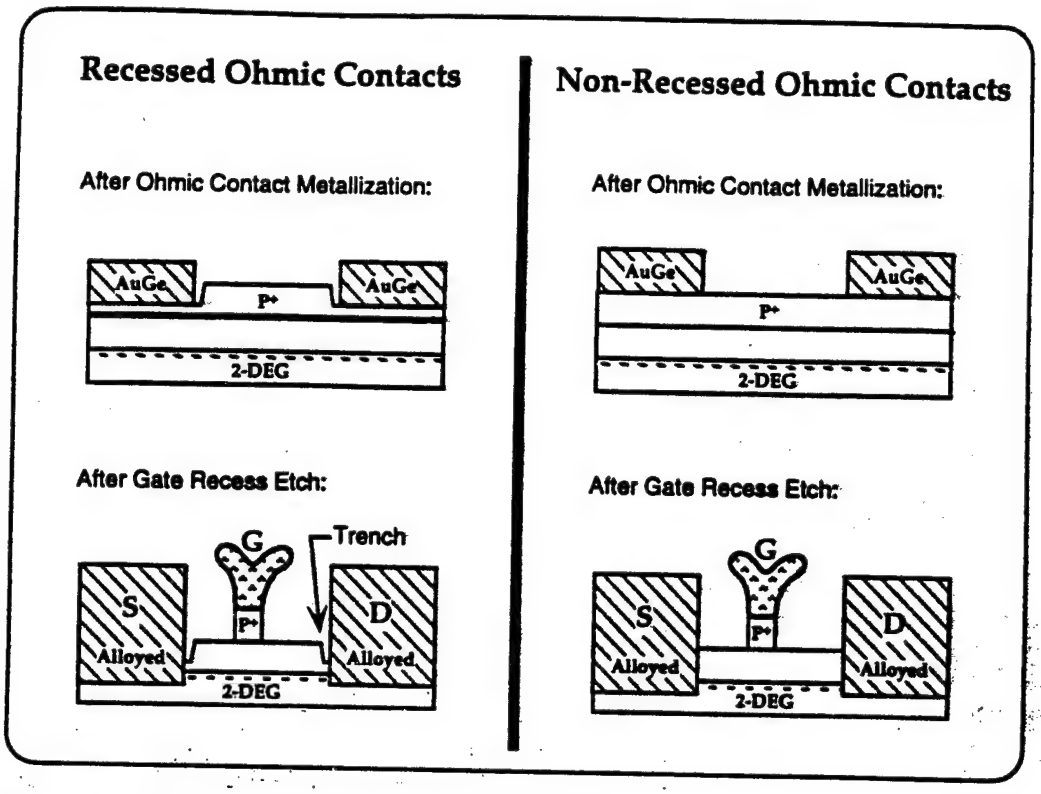


Figure 3.8. Cross section of the JHEMT with recessed ohmic contacts (Left) and non-recessed ohmic contacts (right). The trenching which occurs in the recessed ohmic contact structure effectively i) increases the source and drain access resistance, and ii) limits the maximum channel current.

3.3 Material Characterization

As stressed in the previous two chapters, the large barrier potential of the p^+-gate region in the JHEMT depletes the carriers in the channel. However, as this p^+-gate region is removed the barrier potential is reduced continuously to a minimum value equal to the surface potential of the exposed AlInAs. Hence, carrier depletion in the channel region is

reduced. The increased electron concentration reduces the sheet resistance and thereby the source and drain resistance is reduced. Therefore, it is useful to understand the behavior of the sheet resistance as the access regions are etched.

An additional problem arises when trying to accurately determine the electron mobility and channel sheet charge for a JHEMT structure. The undepleted p^+-gate region cause the Hall mobility and sheet charge to differ from the actual electron mobility and channel sheet charge. First, the holes in the gate region are included in the measured sheet charge, and second, the low mobility of holes in the gate region contribute to the low measured carrier mobility. One suggestion is to remove the p^+-region in order to measure the true electron sheet charge and electron mobility. But, if too little (or too much) is removed, then the measured values are still erroneous and leave unanswered doubts about the quality of the JHEMT material. Therefore, this author developed an experiment in order to verify the transport properties of the material, while (at the same time) optimizing the etch depth necessary to minimize the sheet resistance in the access region.

To profile the JHEMT material, a square sample is prepared with four Indium (In) contacts, one at each corner. The contacts are alloyed through the p^+-region into the channel to simultaneously contact both the gate and the channel layers. The material is profiled by measuring the Hall sheet charge, mobility, and sheet resistance as a function of etch depth. The Hall data is typically measured after ever 20-30Å of material is

removed, until the channel is etched away. Once this material profile of the JHEMT is determined: i) the quality of the material is verified by accurate knowledge of the electron mobility and channel sheet charge, and ii) the sheet resistance profile provides guidance (during the gate recess etch) to obtain the minimum sheet resistance in the source and drain access regions.

The material profile of the double-doped JHEMT (Wafer #V1401) is shown in Figure 3.9. The x-axis of this plot is primarily in time (seconds) and secondarily in units of etch depth (Å) [as calculated from the approximate etch rate known from the slope in Figure 3.5][6] . The plots may be broken up into three regions as shown in the figure. In the first region, the increase in sheet resistance is because the conductance drops slightly as the p^+-region is etched away. This continues until the remaining p^+-surface layer is fully depleted. Across the second region, the surface potential drops with an attendant increase in the channel carrier concentration and electron mobility. The net result of the lower surface potential is lower sheet resistance. In the third region, the p^+-region is completely removed and the barrier layer is slowly etched away. As the barrier-to-spacer thickness ratio decreases, the electron concentration in the channel decreases (see equation [2.9b]) and, subsequently, the sheet resistance increases.

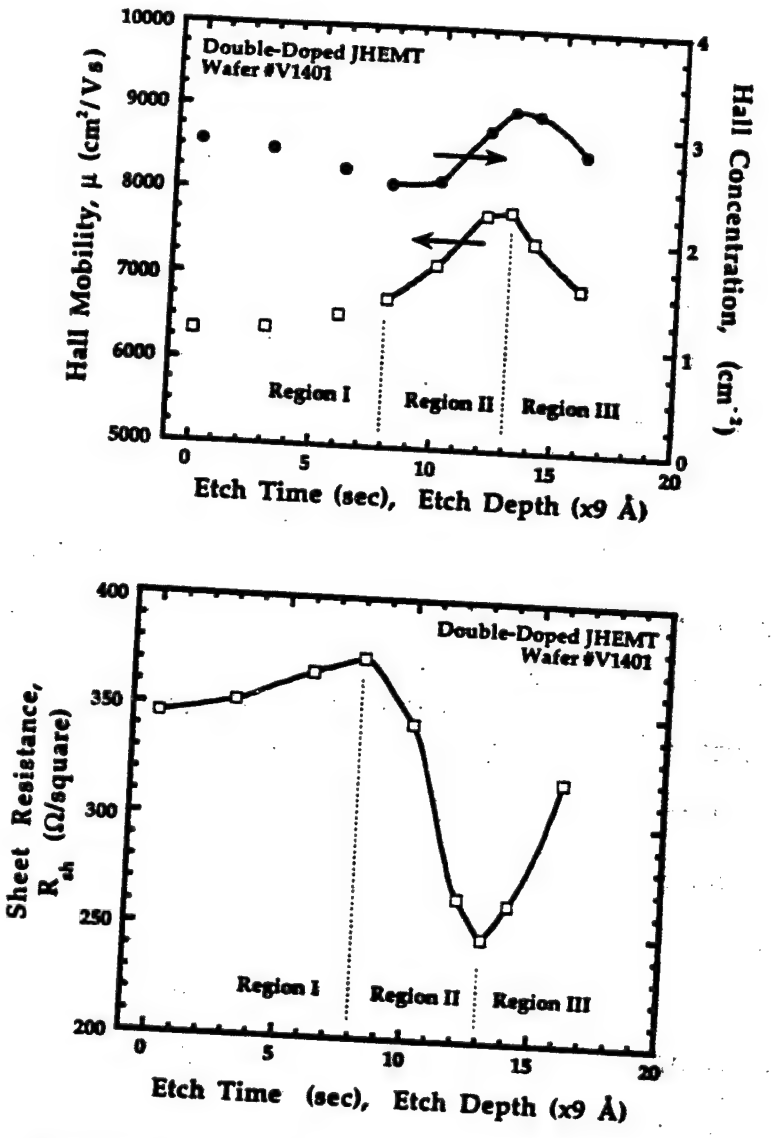


Figure 3.9. The Hall mobility and sheet charge (top), and the sheet resistance (bottom) of a double-doped p⁺-GaInAs/n-AlInAs/GaInAs JHEMT (Wafer V1401). The minimum sheet resistance represents the lowest resistance obtainable in the access regions. The connected portion of the top plot represents channel electron concentration and electron mobility.

3.4 Conclusion

The end-to-end resistance comparison of the T-shaped gate and the triangular-shaped gate suggests that the T-shaped gate must be utilized in order to achieve low gate resistance. The high contact transfer resistance of the regrown ohmic contacts (0.45-0.5Ω-mm) reflects the immaturity of the regrowth technology and is not yet suitable for mm-wave devices. The TLM study of alloyed ohmic contacts suggests that equivalent contact resistance may be achieved with or without recessing the source and drain contacts into the p^+- gate layer. Finally, the material profile of the sheet resistance, mobility and carrier concentration versus etch time provides a means to characterize the material as well as calibrate the required gate recess etch.

References

[1]C.A. Larsen, N.I. Buchan, S.H. Li, G.B. Stringfellow, "GaAs growth Using Tertiarybutylarsine and Trimethylgallium," J. Crystal Growth, Vol. 93, No. 15, 1988.

[2] The doping calibration and optimization was carried out under the guidance of S. Denbaars, by Majid Hashemi and other members of the MOCVD group at UCSB.

[3] BOE is a commonly used term in silicon-based processes, it stands for Buffered Oxide Etch.

[4] An example of this problem is given in S. R. Bahl, and J.A. del Alamo, "Elimination of Mesa-Sidewall Gate Leakage in InAlAs/InGaAs Heterostructures by Selective Sidewall Recessing," IEEE Electron Dev. Lett., Vol. 13, No. 4, pp195-197, April 1992.

[5] Although the ohmic metal must be deposited where low ohmic contact transfer resistance may be achieved to the channel.

[6] Care must be exercised when the precise depth is desired, because each etch time-interval is believed to vary by the time it takes to remove the sample from acid solution to immerse it in the rinse water. For a 45 second, etch this time is negligible, but when intervals are reduced to 2-3 seconds each, (e.g. 0.5 second is 16-25% error each interval which translates into ~10Å error introduced for each data point shown on the plot).

Chapter 4
Single-Doped p+-AlInAs/n-AlInAs/GaInAs JHEMTs

The device structure investigated in this chapter is the p+-AlInAs/n-AlInAs/GaInAs JHEMT. The gate barrier is determined by the work function difference of the neutral p+ gate layer and the 2-DEG, which may be as large as the energy bandgap of the chosen gate material, 1.4 eV for AlInAs. By comparison, the gate barrier height of the Schottky-gate HEMT is 0.6 eV. In the following sections, the performance of both 1μm and 0.2μm gatelength p+-AlInAs/n-AlInAs/GaInAs JHEMTs with regrown ohmic contacts is reported. The fabrication process of both the 0.2μm and 1μm gatelength devices deviated from the mm-Wave process described in Chapter 3. Therefore, the process steps are summarized for each device reported in this chapter.

4.1 1-μm Gatelength p+-AlInAs/n-AlInAs/GaInAs JHEMTs

The p+-AlInAs/n-AlInAs/GaInAs JHEMT structures studied are shown in Figure 4.1. The gate structure consists of 500Å p+-AlInAs (Be:$5x10^{18}cm^{-3}$) followed abruptly (as opposed to graded) by 100Å p+-GaInAs (Be:$3x10^{19}cm^{-3}$). The original epilayer structure was grown by *T. Liu* of Hughes Research Laboratories using a Gas Source MBE. The electron mobility was 7800 and 38,000 cm^2/Vs at 300K and 77K, respectively. Next, the wafer was cleaved into two samples. Sample A went through the regrowth process as shown in Figure 3.1. Sample B was

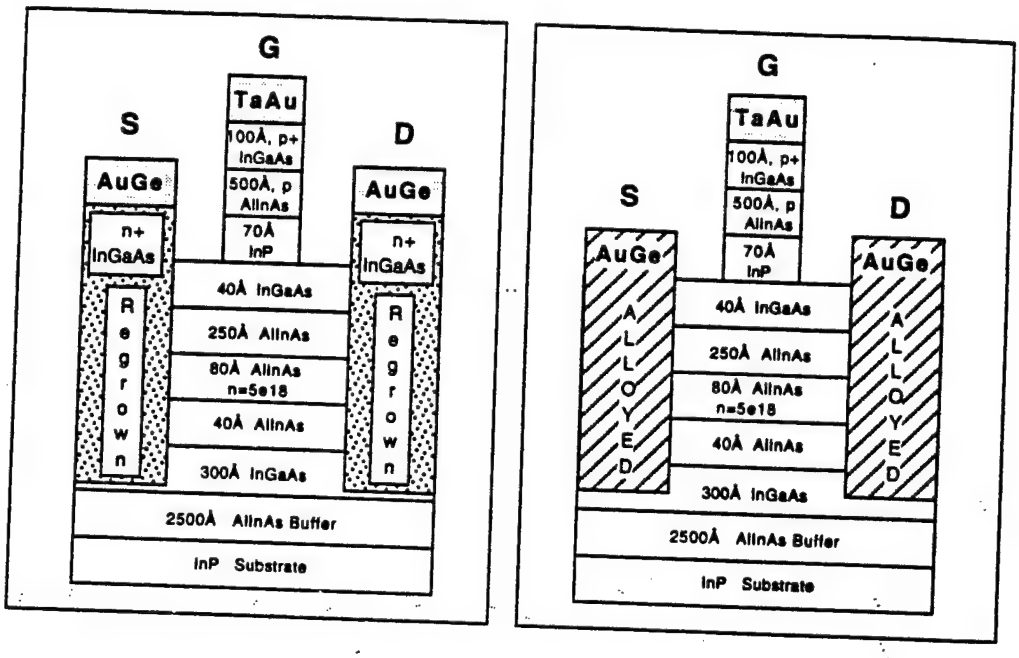


Figure 4.1. 1-μm gatelength p+-AlInAs/n-AlInAs/GaInAs JHEMT structures fabricated. Both regrown ohmic contact (left, sample A-0) and alloyed ohmic contact (right, sample B-370) technologies were utilized. The InP-layer and GaInAs-layer below the gate structure allow the p+-AlInAs gate region to be selectively removed. The p+-GaInAs/p+-AlInAs heterojunction is abrupt and both samples are from the same 2-inch wafer (V645).

placed in dry storage until the regrowth procedure was completed.

Device processing of both samples started with deposition of a refractory gate metal (Ta/Au, 200Å/2300Å) and lift-off to define a 1-μm-long gate using an optical lithography process (see Appendix C). Next, the gate metal was used as the mask for dry etching[1] (CH_4:H_2:Ar) through both the p^+-InGaAs and the p^+-AlInAs. The source-drain mask was then re-aligned and standard AuGe/Ni/Au (1000Å/200Å/1000Å) ohmic contacts were evaporated. Following the lift-off, the samples were patterned for mesa isolation. The isolation mesa was achieved using R.I.E. with chlorine. The standard JHEMT wafer, sample B, was alloyed on a strip heater at 370° C for 3 seconds (sample B-370). Sample A was cleaved and one piece alloyed at 350° C for 3 seconds (sample A-350) while the other piece was left non-alloyed (sample A-0).

The I-V characteristics of 1-μm x 150-μm devices from both sample A-0 and sample B-370 are shown in Figure 4.2. The devices show good pinch-off characteristics and similar transconductance and current density. A plot of g_m and I_{ds} versus V_{gs} (V_{ds}=2-5V) of a 1μm x 150μm device with regrown ohmic contacts (sample A-0) is shown in Figure 4.3. The maximum g_m of the 1-μm gate length devices ranged from 220-240mS/mm.

For sample A-0, with regrown ohmic contact regions, the specific contact resistance and channel sheet resistance were measured to be 0.43 Ω-mm and 300 ohms per square, respectively. Sample B-370 had a specific contact resistance of 0.53 Ω-mm with a channel sheet resistance of 334

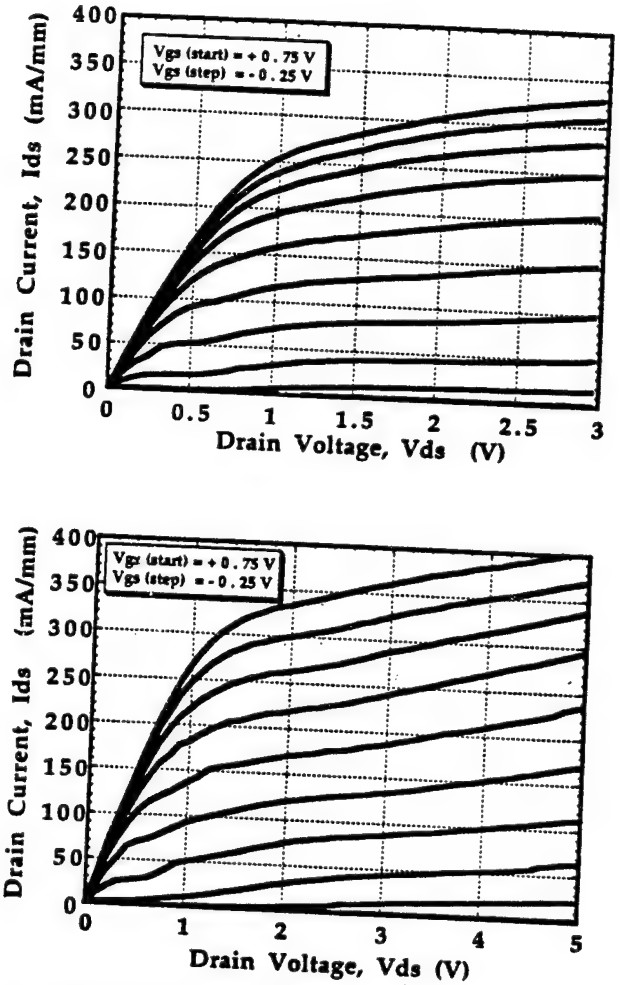


Figure 4.2. DC I-V characteristics of sample A-0 (bottom), and sample B-370 (top). $V_{gs,top} = +0.75V$ and $V_{gs,step} = -0.25V$

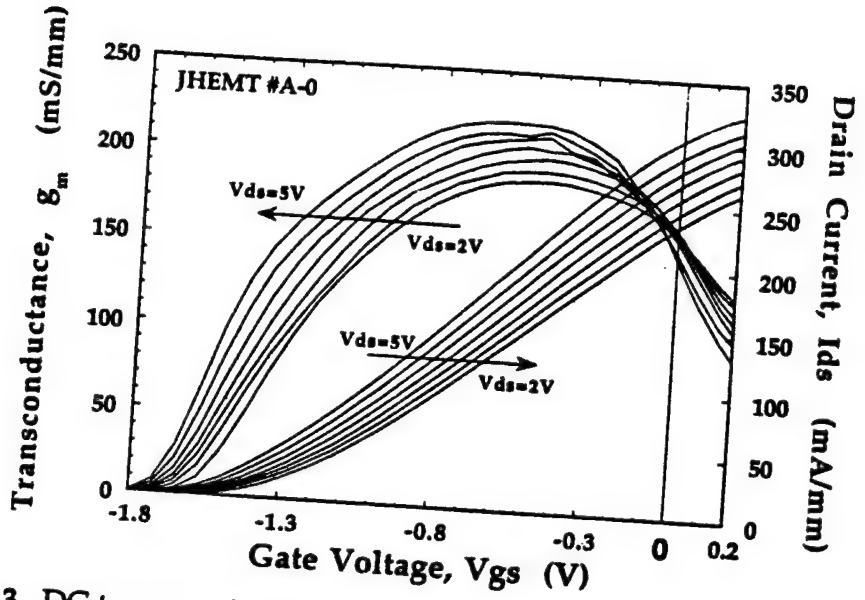


Figure 4.3. DC transconductance and drain current versus gate voltage for the 1μm x 150-μm JHEMT. The drain voltage starts at 2V, increases by 0.5V up to the maximum of 5V.

ohms per square. Thus, the source resistance for sample A-0 and sample B-370 were similar and calculated to be 0.73 Ω-mm and 0.86 Ω-mm, respectively. In addition, the s-parameters were measured from 1-40 GHz for sample A-0, yielding values of 22 GHz and 75 GHz for the (f_τ) and (f_{max}) of the device, respectively, which are typical of HEMTs with a gate length of 1μm.

However, the main advantage of sample A-0 is the uniform, non-alloyed regrown contacts which contribute to the higher breakdown

voltages achieved. The gate-drain diode characteristics of the devices shown in Figure 4.2 are presented in Figure 4.4. The two-terminal gate-drain breakdown voltage of sample A-0 is approximately 31V, which is 40% higher than the 22V breakdown measured for sample B-370. The two-terminal gate-drain breakdown of sample A-350 was 20% lower than sample A-0 but was still better than the gate-drain breakdown of any device from sample B-370.

The two-terminal off-state breakdown has been attributed to impact ionization of electrons injected from the gate into the channel[2]. Further, the ionization rate rises exponentially with increasing electric field[3]. The high two-terminal breakdown voltage obtained for *both* sample A-0 and sample B-370 is attributed to (i) reduced electron injection from the undepleted gate into the channel (which suppresses impact ionization), and (ii) the potential drop across the gate depletion region under reverse bias.

A detailed analysis of the improved breakdown was not undertaken. However, one possible explanation has been proved in a gernalized two-dimensional simulation by Mizuta et al[4]. In this work they analysed the effect of the surface potential on the drain electric field of GaAs MESFETs. An increasing surface potential (increasing negative charge on the surface) relieved the electric field at the gate and enhanced it at the drain. We believe that the drain field can be further enhanced if the contact metal was spiked as is the case for alloyed contacts. This could cause premature breakdown of the gate-drain diode.

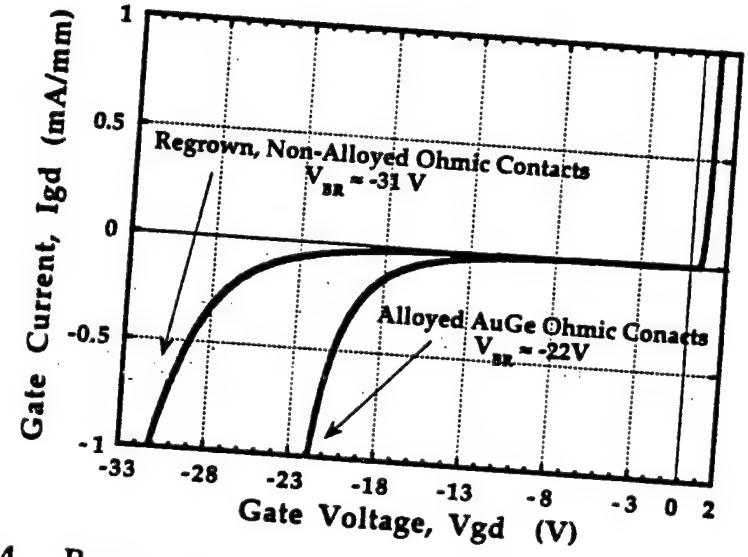


Figure 4.4. Room temperature dc two-terminal gate-drain diode characteristics of the 1-μm gatelength JHEMTs with non-alloyed regrown ohmic contacts (sample A-0) and alloyed ohmic contacts (sample B-370).

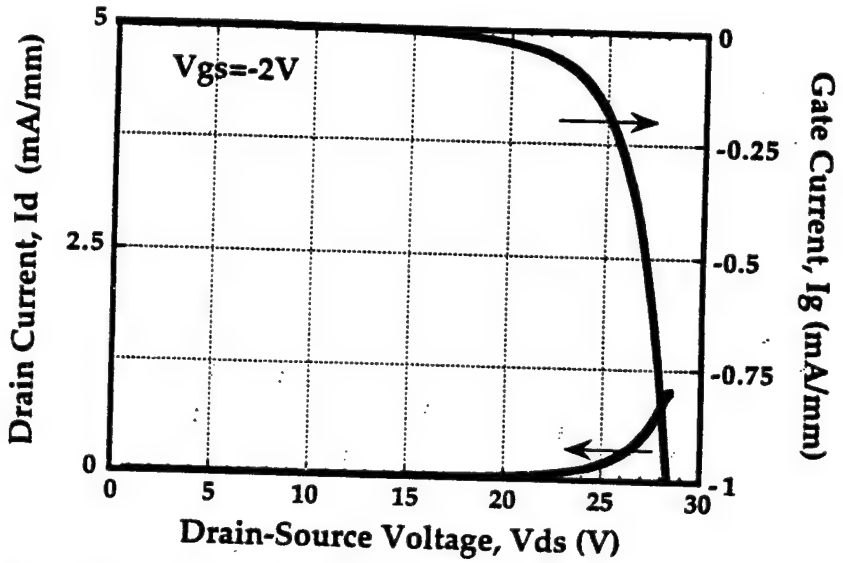


Figure 4.5. Three-terminal off-state breakdown characteristic of the non-alloyed regrown ohmic contact JHEMT (sample A-0). The device is biased into pinch-off, then the drain voltage is increased until the gate current reaches 1mA/mm gate compliance.

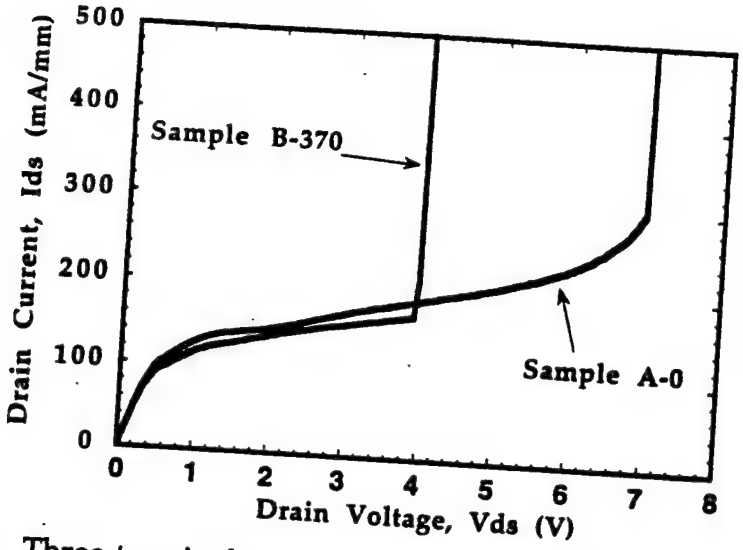


Figure 4.6. Three-terminal on-state breakdown voltage with $V_{gs} = -0.50V$ and $I_{dss} \approx I_{max}/2$. The device is biased at approximately half the full channel current, then the drain voltage is swept until catastrophic breakdown occurs.

The most important breakdown voltage for efficient large signal operation is the three terminal breakdown voltage. We define the *three-terminal off-state breakdown voltage* as the drain voltage, V_{ds}, at which the gate current, I_g, reaches 1 mA/mm under pinch-off conditions. The three-terminal off-state breakdown voltage of a typical device from sample A-0 was 28V and is shown in Figure 4.5. The three-terminal off-state breakdown voltage differs from the two-terminal gate-drain breakdown voltage by the pinch-off voltage applied to the gate electrode:

$$V_{3BV,off} = V_{2BV,gd} - V_{po} \qquad [4.1]$$

This indicates that the three-terminal off-state breakdown is dominated by the same mechanism as the two terminal gate-drain breakdown.

We define the *three-terminal on-state breakdown voltage* as the drain voltage at which catastrophic breakdown occurs when the device is biased at $I_{ds} = I_{dss}/2$. The on-state breakdown voltage characteristic for both sample A-0 and sample B-370 is shown in Figure 4.6. The catastrophic three-terminal on-state breakdown voltage occurs at 4V for sample B-370 and increased to 7V for sample A-0. The source-drain spacing of sample A-0 and sample B-370 were 3.7μm and 4μm, respectively. The shorter source-drain spacing for sample A-0 is due to lateral undercut during the etch prior to regrowth.

The behavior just before catastrophic breakdown occurs for the two samples is different. The drain current of sample B-370 exhibits sharp breakdown behavior, whereas the drain current of sample A-0 exhibits soft breakdown behavior (in the form of slowly increasing drain current) before sharply breaking down. The increase in drain current (over the drain voltage range of 6-7V) for sample A-0 is registered as negative gate current, which is consistent with either electrons (injected from the gate into the channel) or holes (swept from the channel into the gate). Injection of electrons from the gate is unlikely due to the undepleted p^+-gate region. Therefore, the increase in on-state breakdown voltage for the test sample is attributed to suppressed hole current in the channel. This hole current

may originate from (i) impact ionization in the channel when a critical electric field is reached, and/or (ii) hole injection from the drain metal.

In general, the on-state breakdown voltage is less than the off-state breakdown voltage due to the source current which is present when the device is turned on. The current flowing through the channel requires that the current desity ($J = \sigma \cdot E$) be continuous at every point in the channel, even at the metal contacts. In the case of alloyed metal contacts, non-uniformities (e.g. metal spiking) at the drain contact requires the electric field to rise in order for the current density to remain constant. The electric field at the drain contact is important because it sets one of the boundry conditions which determines the electric field throughout the channel. In the case of n^+-regrown contacts, the conductivity in the contact regions increases which lowers the the electric field at the contact. Furthermore, the minority carrier population in the n^+ drain contact layer is low which prevents hole injection from the drain metal. Thus, superior three terminal breakdown characteristics are observed in sample A-0 by utilizing non-alloyed, regrown n^+ contacts.

4.2 0.2μm Gatelength p^+-AlInAs/n-AlInAs/GaInAs JHEMTs

The p^+-AlInAs/n-AlInAs/GaInAs JHEMT structure studied is shown in Figure 4.7. The gate structure features a 500Å p^+-AlInAs ($5x10^{18}$ cm^{-3}) graded over 150Å to a p^+-GaInAs ($3x10^{19}$ cm^{-3}) cap. The 150Å grading is included to reduce the gate contact resistivity. The original epilayer structure was grown by Mark Mondry of UCSB using a Solid

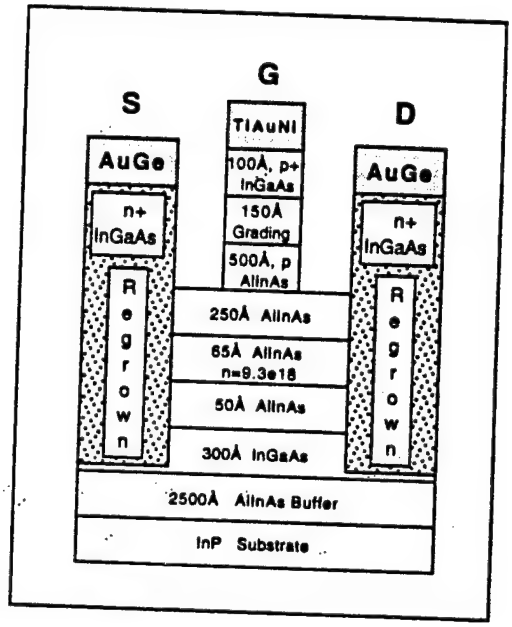


Figure 4.7. Device structure of the 0.2μm gatelength p^+-AlInAs/n-AlInAs/GaInAs JHEMT. The p^+-GaInAs/p^+-AlInAs heterojunction is graded in order to reduce the gate contact resistance.

Source MBE. The electron mobility and sheet density at 300K were 6800 cm^2/Vs and $4.1x10^{12}$ cm^{-2}. The MOCVD regrowth procedure utilized was previously discussed in Section 3.1.

Device processing of the regrown sample begins with the re-alignment of the ohmic level mask to the regrown regions. Then, standard AuGe/Ni/Au ohmic contacts are evaporated. Next, a triangular-shaped 0.2μm gate metal stripe of Ti/Au/Ni is deposited using a single layer resist scheme. The gate metal is then used as the mask for dry etching (CH_4:H_2:Ar) through both the p+ GaInAs and the p+ AlInAs. Following the gate etch, the sample is patterned for isolation and a mesa is etched by RIE with chlorine gas. Finally, the gate pad was electrically isolated from the active region. SEM micrographs of the triangular gate and the final device structure are shown in Figure 4.8, where the regrown ohmic regions and the vertical sidewall of the mesa are noticeable features in the bottom figure.

A plot of g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V) of a 0.2μm x 50μm device is shown in Figure 4.9. The threshold voltage is -3.2V and the full channel current is 450mA/mm . The peak g_m at V_{ds}=1.5V is 250mS/mm and the maximum g_m is 300mS/mm at V_{ds}=2V. The low transconductance is attributed to the high gate to channel separation and the transconductance compression near -1V is due the onset of parallel conduction in the AlInAs donor layer[5]. The threshold voltage of the JHEMT is established by the thickness of the barrier layer and increases with the back depletion[6] into the p^+-gate region.

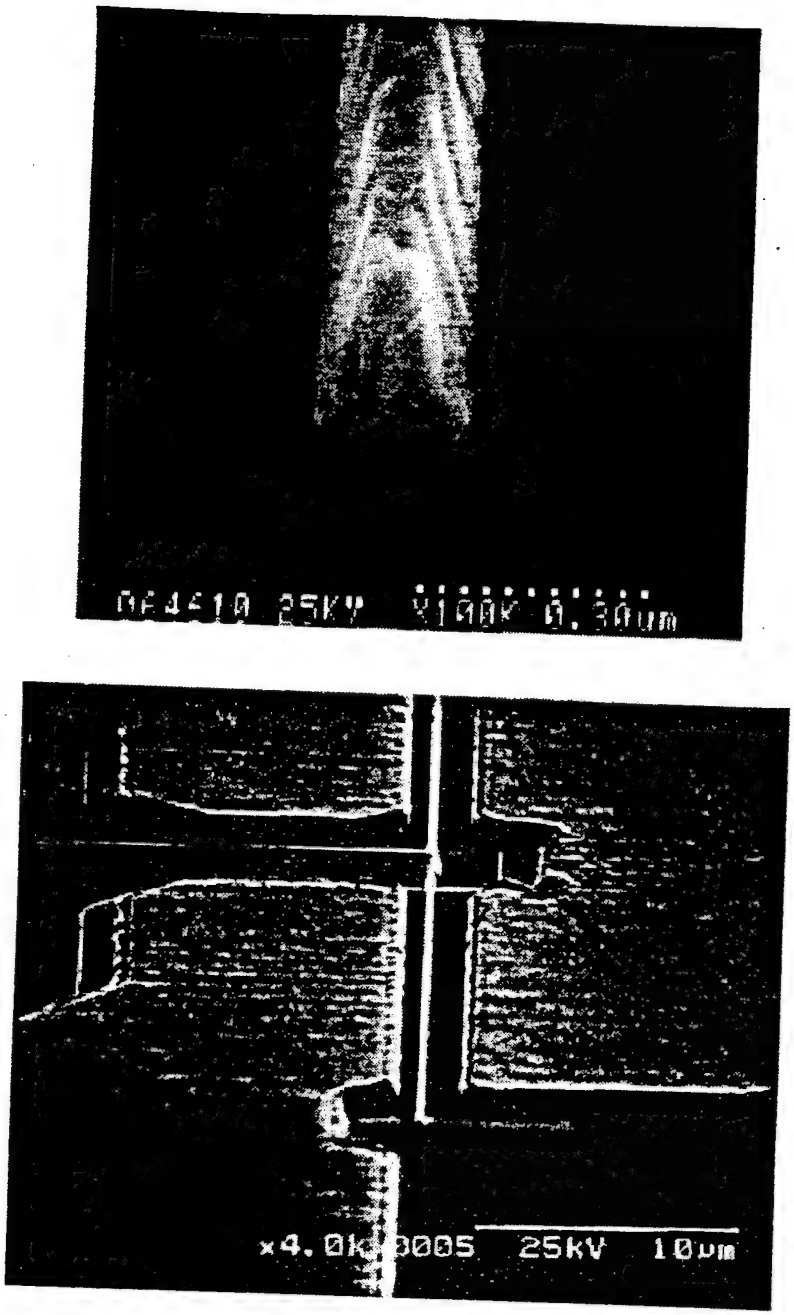


Figure 4.8. SEM micrographs of the 0.2µm triangular-shaped gate (top) and the device layout of the 0.2µm p^+-AlInAs/n-AlInAs/GaInAs JHEMT(bottom). In the layout view, the regrown regions are clearly seen as is the dry-etched, vertical sidewall of the mesa.

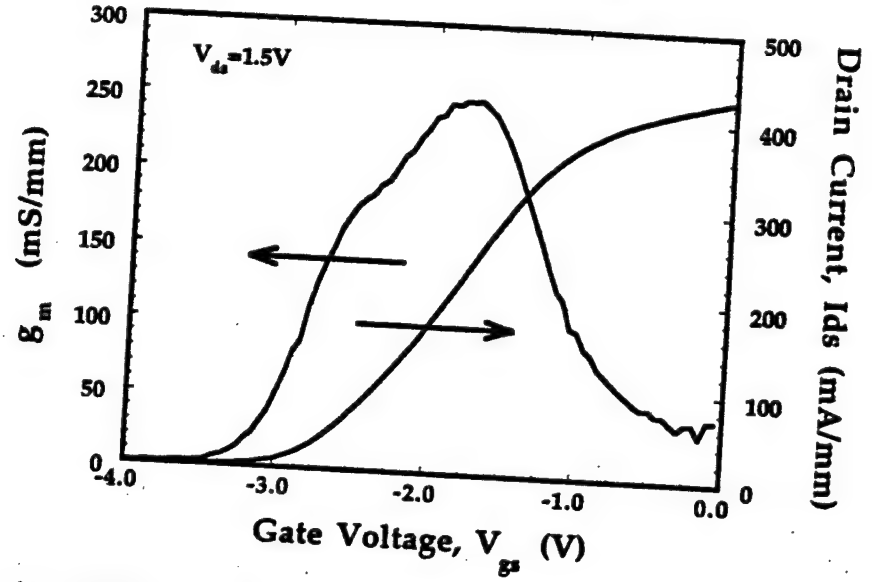


Figure 4.9. DC g_m and I_{ds} vs V_{gs} for the 0.2μm x 50-μm JHEMT. The compression of the transconductance near $V_{gs} = -1V$ is due to parallel conduction in the AlInAs donor region. The high threshold voltage is the result of the thick barrier layer and back depletion into the p^+-gate region.

The contact transfer resistance and channel sheet resistance were measured to be approximately 0.5 Ω-mm and 330 ohms per square, respectively. The source and drain resistance is determined from forward bias gate-diode s-parameter measurements to be 14.6Ω (0.73 Ω-mm) and 20Ω (1Ω-mm). The parasitic resistance is dominated by the effective contact transfer resistance which was measured from TLM patterns to be

used.

A plot of the gate-drain diode characteristic is shown in figure 4.10. The two terminal reverse breakdown voltage is -19V. The high breakdown behavior is similar to the 1μm gatelength devices discussed in the previous section. The three-terminal off-state breakdown voltage is 15 volts and, once again, differs from the two-terminal reverse breakdown voltage by the applied pinch-off voltage. The three-terminal on-state breakdown characteristic is shown in Figure 4.11. The three-terminal on-state breakdown voltage is 5.2V for a source-drain spacing of 2.7μm compared to 7V for the 1μm gatelength JHEMT with a spacing of 3.7μm.

The microwave S-parameters were measured on-wafer using a Wiltron 360 Network Analyzer. A plot of gain versus frequency (V_{ds}=1.4V, V_{gs}=-2.4V) is given in Figure 4.12 revealing the (f_τ) and (f_{max}) of 0.2μm gatelength device to be 62GHz and 105GHz, respectively. In addition, the S-parameters were measured versus drain bias from 0.8V to 1.8V at V_{gs}=-1.3V. The bias dependence of RF cut-off frequencies for the 0.2μm JHEMT is shown in Figure 4.13. The peak (f_τ) is 62GHz at V_{ds}=1.5V and the peak (f_{max}) is 108GHz at V_{ds}=1.8V. The cut-off frequency trends are consistent with the analysis of Hughes and Tasker[7].

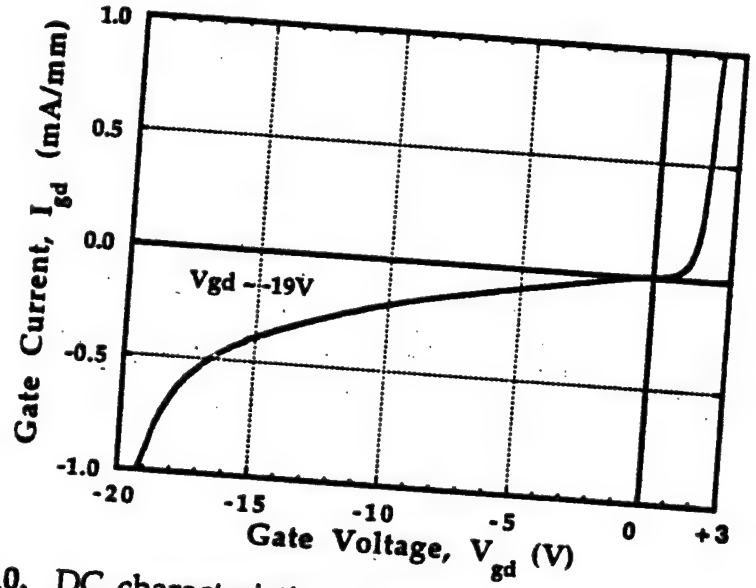


Figure 4.10. DC characteristics of the gate-drain diode for the 0.2μm gatelength JHEMT.

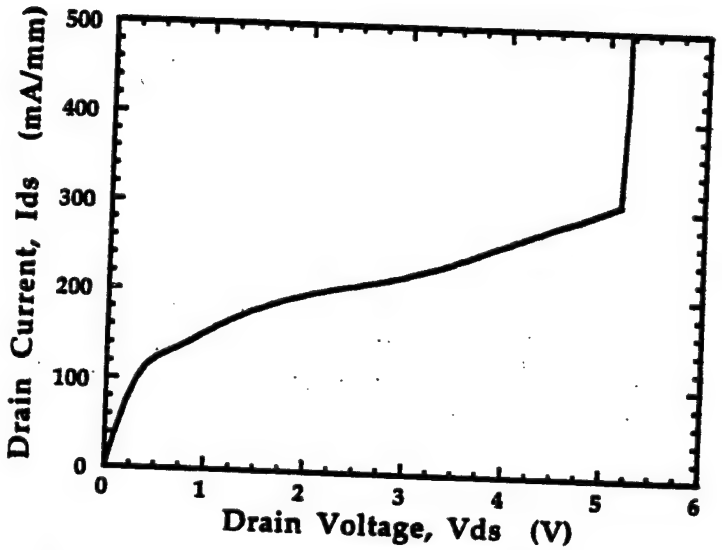


Figure 4.11. Three-terminal on-state breakdown voltage of the 0.2μm gatelength JHEMT. The source-drain spacing of this structure is 2.7μm. The soft breakdown region shows the onset of carrier multiplication.

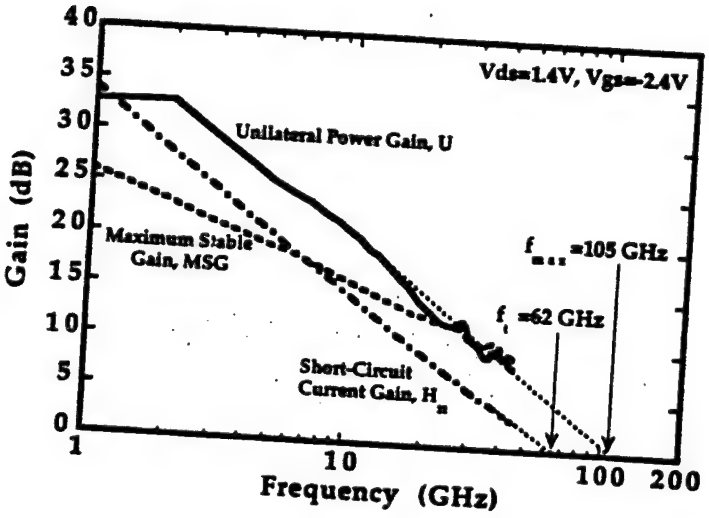


Figure 4.12. RF gain versus frequency for the 0.2μm gatelength JHEMT.

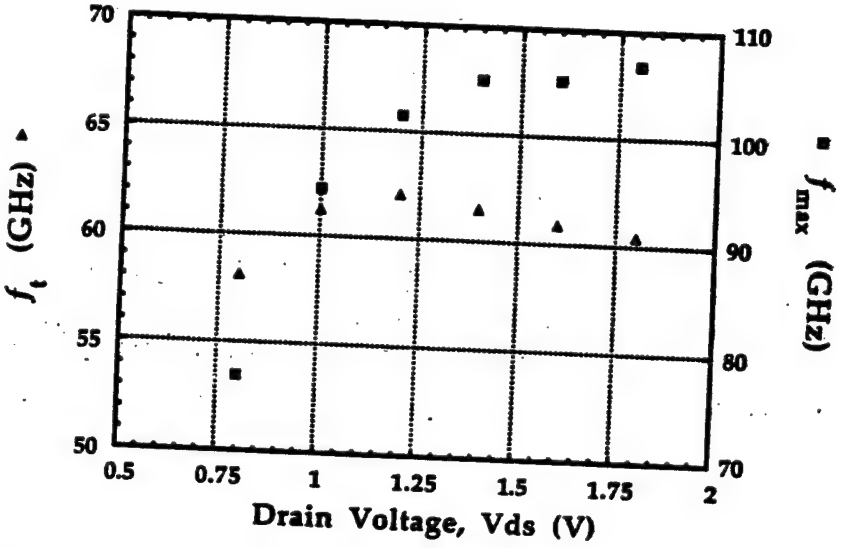


Figure 4.13. Small signal cut-off frequencies, (f_t) and (f_{max}), versus drain bias of the 0.2μm P+-AlInAs gate JHEMT.

4.3 Synopsis of the p+-AlInAs/n-AlInAs/GaInAs JHEMT

The high gate potential of the p+-AlInAs/n-AlInAs/GaInAs JHEMT is reflected in the high forward turn-on voltage seen in Figure 4.10. This is desirable for enhancement-mode JHEMTs which are suitable for high speed digital and single power supply wireless systems. Using our current regrowth technology, superior breakdown characteristics were demonstrated. However, the high contact transfer resistance obtained translates into a high parasitic transit delay (through the source and drain resistance) and must be reduced to be effective in mm-wave device technology. In future designs, the aspect ratio must be improved in order to both achieve improved RF performance and suppress parallel conduction in the AlInAs. The need to reduce the gate-channel separation is also evident from the low intrinsic gate capacitance (0.5pF/mm), which is half the typical high frequency gate capacitance design rule of 1pF/mm[8].

In the Chapter 5, the following aspects are addressed. First, the gate resistance is reduced by utilizing a T-shaped gate (reducing the metal end-to-end resistance) and utilizing a gate material, by which low contact resistivity contacts may be achieved. Second, the source and drain resistance and associated parasitic delays are reduced by (i) lowering the contact transfer resistance, (ii) lowering the channel resistance, and (iii) scaling the device geometry. Third, the aspect ratio is improved by optimizing the epitaxial-layer design and by reducing the back depletion into the gate region. Finally, the threshold voltage is reduced by reducing

the barrier layer thickness.

References

[1] J. Werking, J. Schramm, C. Nguyen, E.L. Hu and H. Kroemer, "Methane Hydrogen-Based Reactive Ion Etching of InAs, InP, GaAs, and GaAs," Appl. Phys. Lett, Vol. 58, No. 18, pp.2003-2005, May 6, 1991.

[2] S.R. Bahl, J.A. del Alamo, J. Dickman, and S. Schildberg, "Off-State Breadown in InAlAs/InGaAs MODFETs," IEEE Trans. Elect. Dev., Vol. 42, No.1, Jan 1995.

[3] S.M. Sze, *Physics of Semiconductor Devices*, John Wiley Publishing, p. 45, 1981.

[4] H. Mizuta, K. Yamaguchi, and S. Takahashi, "Surface Potential Effect on Gate-Drain Avalanche Breakdown in GaAs MESFET's," IEEE Trans. ELectron Dev., Vol ED-34, No. 10, p. 2027, 1987.

[5] K. Lee, M.S. Shur, T.J. Drummond, and H. Morkoc, "Parasitic MESFET in (Al, Ga) As/GaAs Modulation Doped FETs and MODFET Charcterization," IEEE Trans Electron Dev., Vol . ED-31, pp. 29-35, Jan 1984.

[6] For example, see equation [2.27].

[7] B. Hughes and P.J. Tasker, "Bias Dependence of the MODFET Intrinsic Model Element Values at Microwave Frequencies," IEEE Trans. on Electron Devices, Vol. 36, No. 10, October 1989.

[8] B. Hughes and P. Tasker, "Scaling of Parasitics in mm-Wave MODFETs," SPIE, Vol. 1288, Pg. 227, 1990.

Chapter 5
p^+-GaInAs/n-AlInAs/ GaInAs JHEMTs

I. Single-Doped p^+-GaInAs/n-AlInAs/ GaInAs JHEMTs

In the first half of the chapter, the performance and behavior of the single-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT is presented. The advantages of the p^+-GaInAs gate electrode over a p^+-AlInAs gate electrode are examined. Next, a summary of the single-doped p^+-GaInAs/n-AlInAs/GaInAs wafers grown is given. The material profile of the devices reported in this chapter is also provided. The dc characteristics of the 0.2μm gatelength p^+-GaInAs/n-AlInAs/GaInAs JHEMT are presented along with evidence to support thermionic field emission as the dominant current flow mechanism in the forward diode characteristics. Then, the threshold voltage uniformity of the p^+-GaInAs/n-AlInAs/GaInAs JHEMT is reported followed by the influence of the barrier layer thickness on the threshold voltage. Finally, the microwave performance is examined including small-signal model parameters and noise performance at 12GHz.

5.I.1 Layer Structure

The layer structure of the single-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT is similar to the p^+-AlInAs/n-AlInAs/GaInAs JHEMT reported in the previous chapter if the p^+-AlInAs layer is removed from the gate region. This subtle change has far reaching consequences

including (i) lower gate resistance, (ii) reduced threshold voltage, and (iii) a more flexible fabrication process. The following sub-sections look at the advantages of removing the p+-AlInAs from the JHEMT structure and summarize the electrical quality of the single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT material grown.

5.I.1.1 Material Advantages

The band diagrams of the p+-GaInAs/n-AlInAs/GaInAs JHEMT and the p+-AlInAs/n-AlInAs/GaInAs JHEMT are overlaid in Figure 5.1. First, by the removing the p+-AlInAs, the valence band discontinuity at the p+-GaInAs/p+-AlInAs heterojunction is eliminated. This reduces the gate contact resistivity and, subsequently, the gate contact resistance. Recall from Figure 2.8, the lower contact resistivity is most significant at short gatelengths.

Second, the thickness of the gate layer may be reduced by eliminating the p+-AlInAs from the gate region. This, consequently, allows the gate recess etch to be achieved using wet etching as the gate undercut is reduced. Subsequently, the triangular-shaped gate used in the previous chapter (see Figure 4.8) may be replaced by a T-shaped gate, which has one-third the metal end-to-end resistance. Recall from Chapter 2, this directly results in one-third the RF gate metal resistance. Therefore, the total gate resistance can be reduced by utilizing a single thin, p+-GaInAs gate layer.

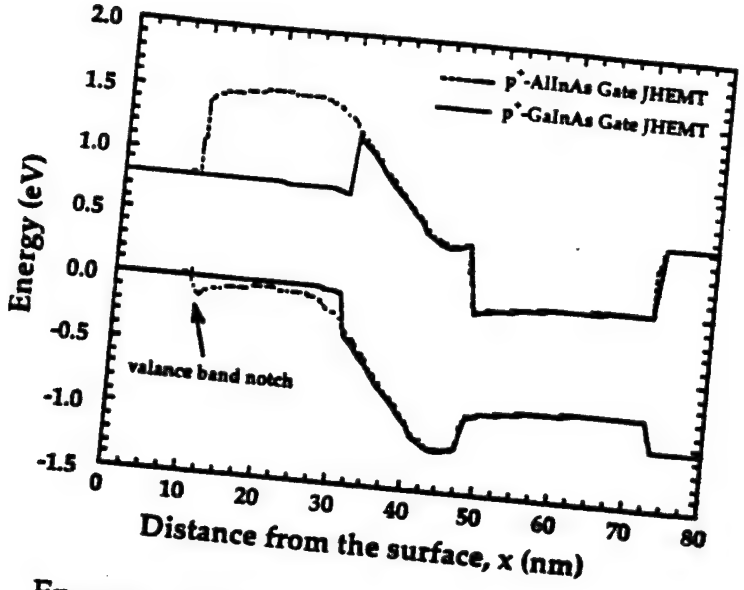


Figure 5.1. Energy band diagram comparing the p+-GaInAs/n-AlInAs/GaInAs JHEMT with the p+-AlInAs/n-AlInAs/GaInAs JHEMT. The valance band notch is eliminated at the expense of a lower electron barrier.

Third, the ohmic contacts to the channel may be alloyed through the thin p+-GaInAs gate layer to obtain lower source and drain parasitic resistance. In the p+-AlInAs/n-AlInAs/GaInAs JHEMT, the gate layers were too thick to achieve low contact transfer resistance to the channel. Thus, the ohmic contact regions were regrown unless additional etch-stop layers were added to the structure.

Finally, the p+-GaInAs layer may be doped to much higher values than p+-AlInAs. The p+-GaInAs layers grown for the JHEMTs in this chapter were doped from $3x10^{19}$ to $1x10^{20}$ cm^{-3} using beryllium (Be) which acts as an acceptor. In addition to a lower gate contact resistance,

higher acceptor doping results in less back depletion, and therefore a lower threshold voltage. First, the back depletion from modulation doped layers into the gate region is inversely proportional to the acceptor doping in the gate layer (according to equation [2.19]). The back depletion effectively increases the gate-to-channel separation, which degrades the aspect ratio of the device. Therefore, by simply increasing the acceptor doping in the gate region from $5x10^{18}$ cm^{-3} to $1x10^{20}$ cm^{-3}, the aspect ratio of the JHEMT is improved by 45 percent[1]. Second, the second-term in the derived expression for threshold voltage (equation [2.23]), is inversely proportional to the acceptor doping in the gate. This term is negligible if the gate is doped extremely high (e.g. $1x10^{20}$ cm^{-3}), and the threshold voltage is less negative.

5.I.1.2 Material Characterization

The single-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT structure is shown in the top of Figure 5.2. All four structures were grown by *T. Liu* of Hughes Research Laboratories. The thickness chosen for the gate region was 200Å for all the wafers studied. Further the donor layer sheet charge was constant at $6x10^{12}cm^{-2}$, but the thickness of the donor layer was varied. The table given in the middle of the figure shows the variations in gate-layer doping, and layer thicknesses of the four wafers studied. For each of the gate layers studied, the depletion due to the surface potential plus the back depletion was less than 100Å[2]. The Hall data of the four p^+-GaInAs/n-AlInAs/GaInAs JHEMT wafers is tabulated in the bottom of Figure 5.2. The accuracy of the tabulated sheet resistance

Layer	*Name*	*Thickness*	*Material*	*Doping*
1	Gate	200Å	GaInAs	N_A
2	Schottky	t_2	AlInAs	
3	Donor	t_n	AlInAs	$n_d=N_d t_n$
4	Spacer	t_1	AlInAs	
5	Channel	t_{ch}	GaInAs	
6	Buffer	2500Å	AlInAs	
	Substrate		InP	

	Tencor	t_2	t_n	t_1	t_{ch}	n_d	N_A
Wafer	Ω/sq	Å	Å	Å	Å	cm^{-2}	cm^{-3}
V1306	344	140	50	17	400	6E12	1E20
V1307	441	100	50	17	400	6E12	1E20
V1308	387	100	δ	17	400	6E12	1E20
V1351	—	140	50	17	400	6E12	3E19

HALL	R_{sh}	μ_e	n_s
Wafer	Ω/sq	cm^2/Vs	cm^{-2}
V1306	254	9941	2.5E12
V1307	291	8510	2.5E12
V1308	280	7500	3.0E12
V1351	322	10140	1.9E12

Figure 5.2. Table Summary of the Single-Doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT showing the basic layer structure (top), layer structure parameters (middle), and the measured Hall data (bottom).

is within 10% of the actual value sheet resistance measured on the device wafer.

As shown in the hall measurements for thin spacer layers, the mobility is lower for a planar-doped donor region versus a distributed-doped donor layer. A plot of room temperature electron mobility versus spacer width (for both planar-doped and uniformly-doped donor layers) is shown in Figure 5.3, where the JHEMT mobilities are comparable with the mobilities reported by Nguyen and co-workers[3]. Further, a maximum sheet charge ($2.5 \times 10^{12} cm^{-2}$) and low sheet resistance (less than 300Ω/sq) of the JHEMT structure are achieved after careful removal of the p^+-GaInAs layer which lowers the surface potential.

The material profile of the single-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMT is shown in Figure 5.4. The minimum sheet resistance obtainable in the access regions is determined by the minimum value in the sheet resistance profile, which is 290Ω/sq. The steep rise in the sheet resistance after this minimum value indicates the complete removal of the gate layers and the on-going removal of the barrier layer[4]. This is accompanied by the decline in both electron sheet concentration and electron mobility as shown in the material profile.

5.I.2 DC Characteristics

5.I.2.1 Three-Terminal Characteristics

The width of the single-doped p^+-GaInAs/n-AlInAs/GaInAs JHEMTs studied were 50 and 100μm. The record results from devices

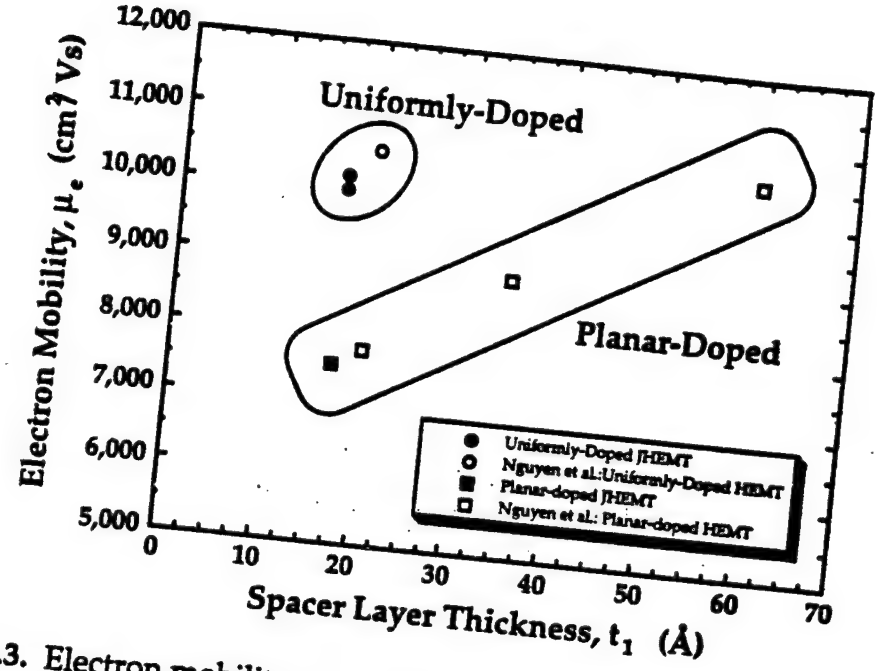


Figure 5.3. Electron mobility dependence on the spacer layer thickness for both distributed-doped donor layers and planar-doped donor layers. (For Nguyen: see reference [3].)

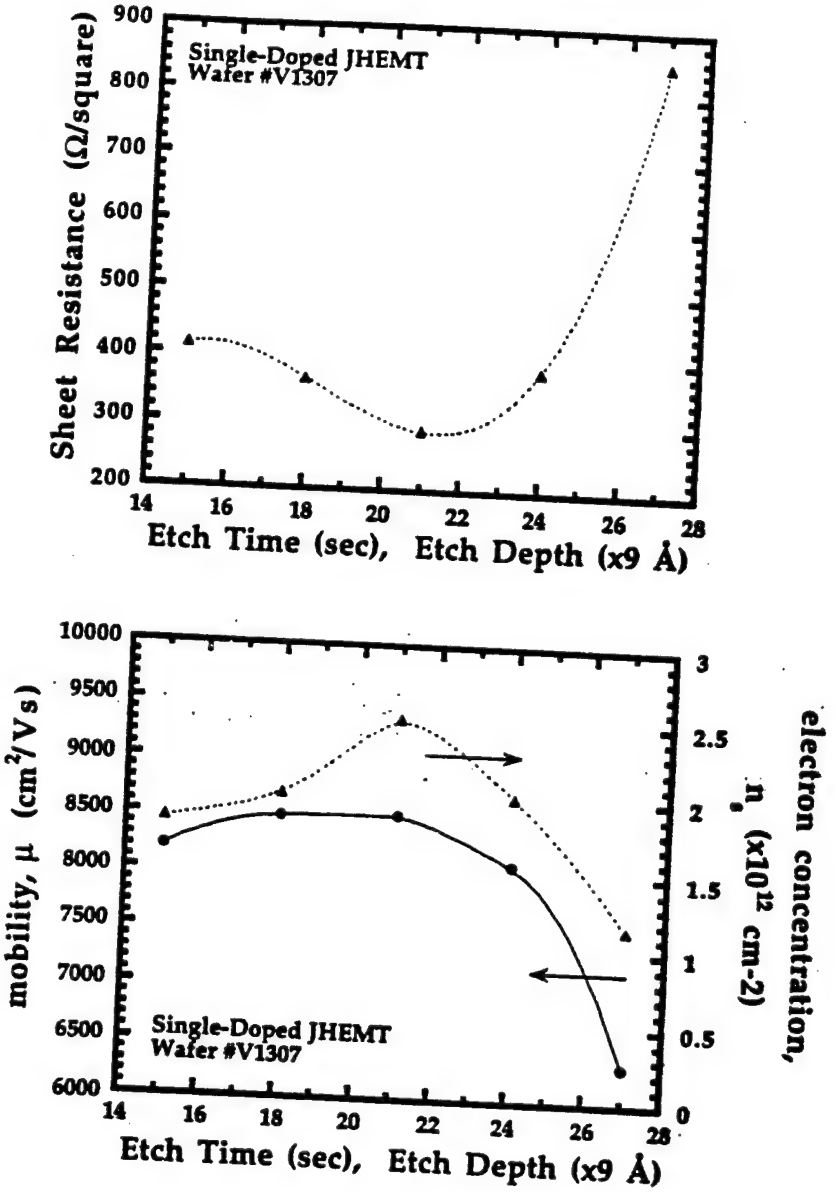


Figure 5.4. Material profile for the p⁺-GaInAs/n-AlInAs/GaInAs JHEMT (wafer #V1307). The sheet resistance (top), and the electron mobility and sheet concentration (bottom) are shown.

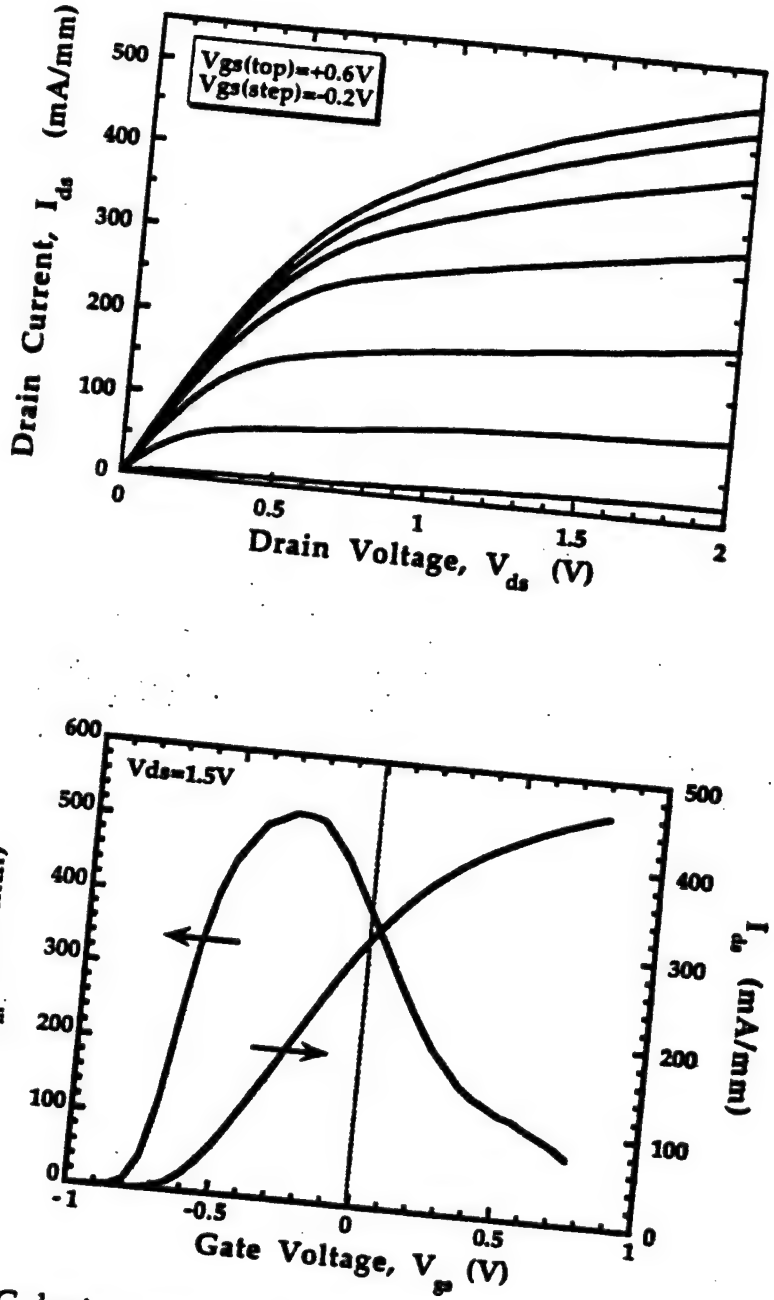


Figure 5.5. DC device characteristics: I_{ds} vs V_{ds} (top), and g_m and I_{ds} vs V_{gs}, (bottom) of the single-doped JHEMT (Wafer #V1307).

with 0.2μm gatelength are present below. Plots of I_{ds} versus V_{ds}, and g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V) are shown in Figure 5.5. The full channel current and dc transconductance shown for a 100μm device is 460mA/mm and 520mS/mm, respectively. The improved dc transconductance, over p+-AlInAs gate JHEMTs, results from reduced source resistance as well as the high aspect ratio.

The source-drain and gate-source spacings are 2μm and 0.5μm, respectively. The contact transfer resistance and channel sheet resistance were measured to be approximately 0.4 Ω-mm and 300 ohms per square, respectively. The source and drain resistance is determined from forward bias, three terminal gate-diode s-parameter measurements to be 5.5Ω (0.55 Ω-mm) and 7.5Ω (0.75Ω-mm) for the 100μm wide device.

5.I.2.2 Two-Terminal Characteristics

Reverse Gate-Drain Diode

A plot of the reverse gate-drain diode characteristic is shown in Figure 5.6. The two-terminal gate-drain breakdown voltage is -10V for a 1.5μm gate-drain spacing. The lower two-terminal breakdown voltage, compared to the 0.2μm gatelength p+-AlInAs JHEMT reported in Chapter 4, is attributed to (i) a shorter gate-drain spacing resulting from scaled device dimensions, and (ii) the elimination of the potential drop across the gate depletion region by removal of the p-AlInAs.

Forward Gate-Drain Diode

A plot of the forward gate-drain I-V characteristic is shown in Figure 5.7. The room temperature forward turn-on voltage, defined at

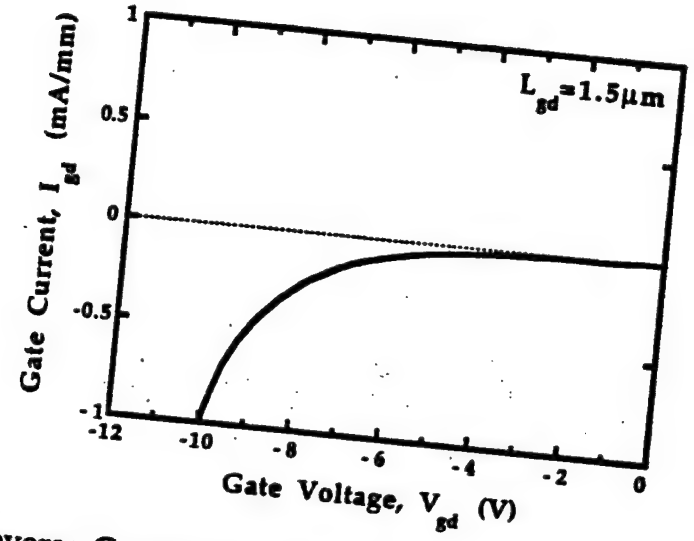


Figure 5.6. Reverse Gate-Drain Diode Characteristic of 100μm wide p+-GaInAs/n-AlInAs/GaInAs JHEMT.

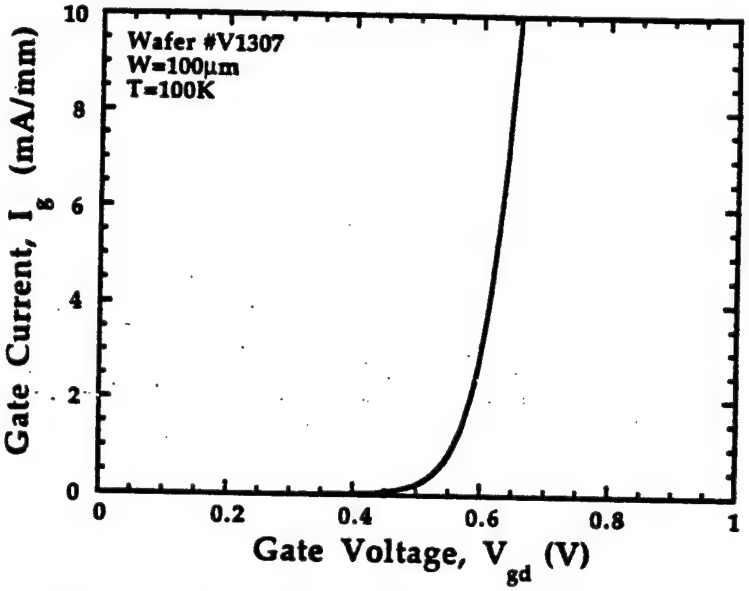


Figure 5.7. Forward gate-drain diode characteristic of the p^+-GaInAs/n-AlInAs/GaInAs JHEMT.

1mA/mm gate current, is 0.57V. From the band diagram of the p+-GaInAs/n-AlInAs/GaInAs JHEMT in Figure 5.1, this value is considerably lower than the electron barrier (1.3eV) at the p+-GaInAs gate layer/AlInAs barrier layer hetero-interface. Therefore, an analysis of the forward diode characteristics was undertaken.

Forward Gate-Drain Current Model

The possible current flow mechanisms in the p+-GaInAs/n-AlInAs/GaInAs JHEMT diode under forward bias are shown in Figure 5.8. The four possible components of current are (a) thermionic emission electron current,(J_{te}), over the barrier (b) thermionic field emission electron current,(J_{tfe}), at energies below the peak of the barrier, (c) recombination current,(J_{rec}), by the presence of traps at the p+-GaInAs/AlInAs hetero-interface, and (d) thermionic emission hole current,(J_h). The interface-trap density is assumed small, and the recombination current is neglected. Also, the hole current is also assumed negligible for voltages much smaller than the hole barrier. Therefore, the total diode current is approximately equal to:

$$J_{tot} = J_{te} + J_{tfe} \qquad [5.1]$$

The total current density from the channel to the gate of the p+-GaInAs/n-AlInAs/GaInAs JHEMT diode is given by:

$$J_{tot} = \int_{v_0}^{\infty} q \cdot v_z \cdot T(v_z) \cdot dn \qquad [5.2]$$

where q is the fundamental electron charge, v_z is the electron velocity perpendicular to the heterojunction, $T(v_z)$ is the transmission probability across the gate potential (i.e. the gate barrier), and dn is the density of

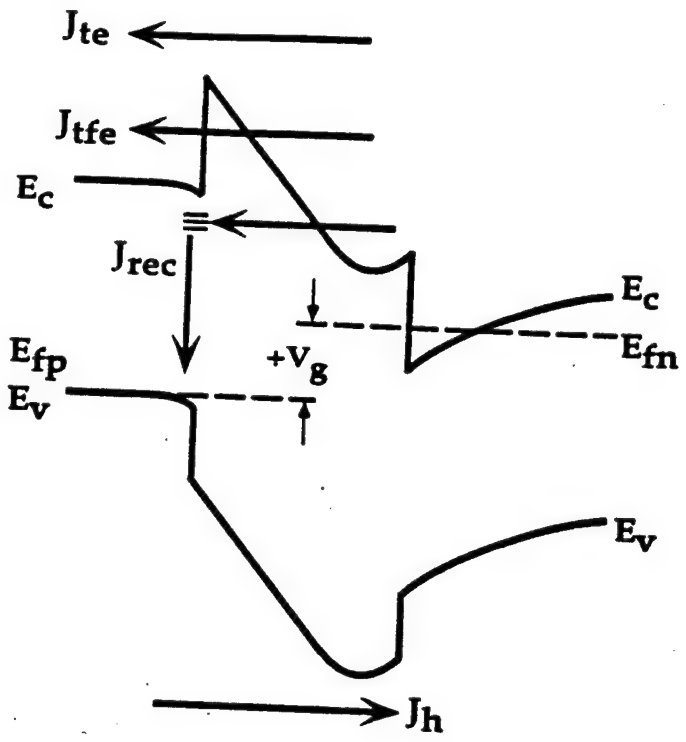


Figure 5.8. Current flow mechanisms in the forward biased p+-GaInAs/n-AlInAs/GaInAs JHEMT gate diode.

electrons with perpendicular velocity between v_z and $v_z + dv_z$. The lower limit of integration, v_0, is the initial electron velocity referenced to the bottom of the conduction band in the channel. The transmission probability across the gate barrier (or gate potential), $T(v_z)$, is calculated by numerically solving the Schrodinger Wave Equation using the propagation matrix (P-matrix)[5]. The P-matrix formalism is extremely useful for electrons being scattered by a non constant potential, which in this particular case is the gate potential.

The gate potential used in the calculation was calculated using Bandprof[6], which provides a self-consistent numerical solution of both Poisson's Equation and the Schrodinger Wave Equation. The conduction band as a function of the applied gate bias is given in Figure 5.9, where the energy reference is the conduction band in the channel at the AlInAs spacer layer/GaInAs channel layer hetero-interface, E_{co}. To calculate the current at each gate bias, the non-constant potential (i.e. the conduction band) was broken into a series of infinitesimal, constant potentials as shown in Figure 5.10, where the selected energy reference is E_{co} as previously defined. The P-matrix is readily calculated for the multi-barrier structure and, subsequently, the transmission probability is found. The interested reader is directed to Appendix E, where the program code used to calculate the transmission probablity is given.

The transmission probability across the gate barrier for the three gate potential (given in Figure 5.9) is shown in Figure 5.11. The plot indicates that there is high probability for electrons to tunnel through the triangular potential barrier. The ensemble of electrons which tunnel through the barrier comprise the thermionic field emission current, J_{tfe}. Figure 5.12 shows the calculated current-voltage (semi-log) characteristic of the p+-GaInAs/n-AlInAs/GaInAs JHEMT gate diode. The plot shows that the total current density is dominated by the tunneling current through gate barrier at gate voltages less than 1V. This was experimentally verified by low temperature diode measurements. The current is normalized to the gate width and plotted against the measured

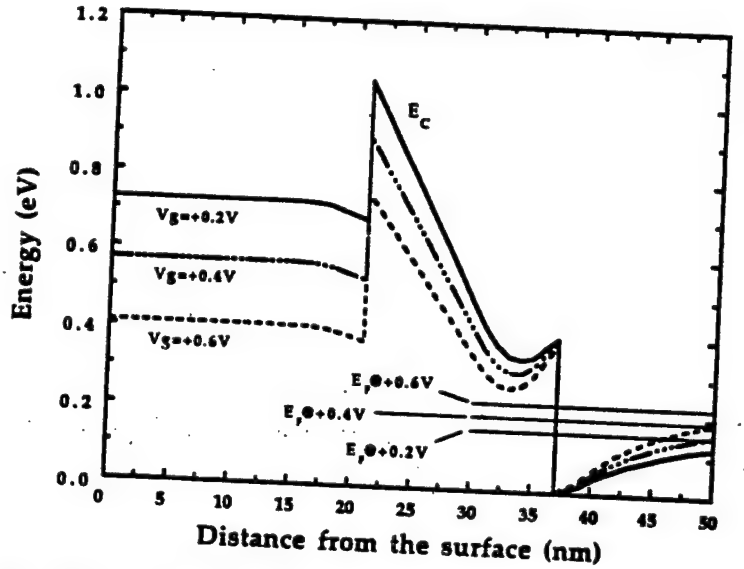


Figure 5.9. Conduction band under forward bias (Vg=+0.2, 0.4, 0.6V). The Fermi Level moves higher into the conduction band as more charge is induced in the channel.

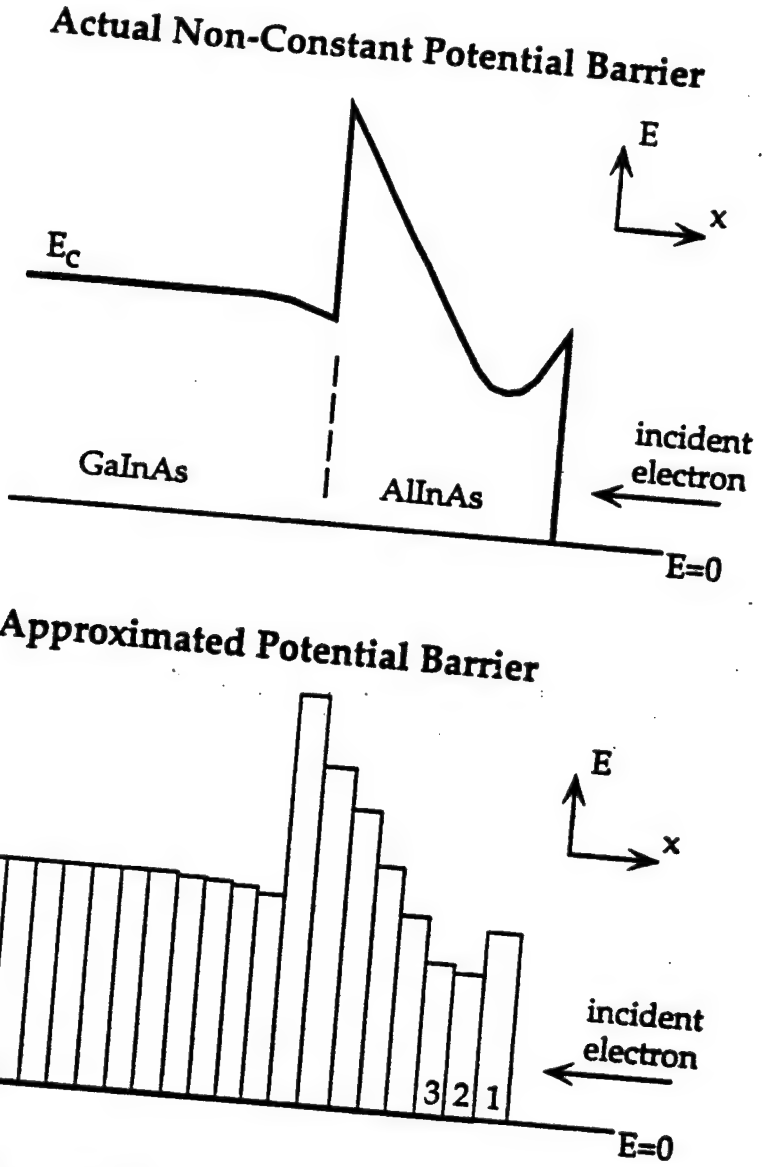


Figure 5.10. Composite barrier approximation of the gate potential for the p^+-GaInAs/n-AlInAs/GaInAs JHEMT.

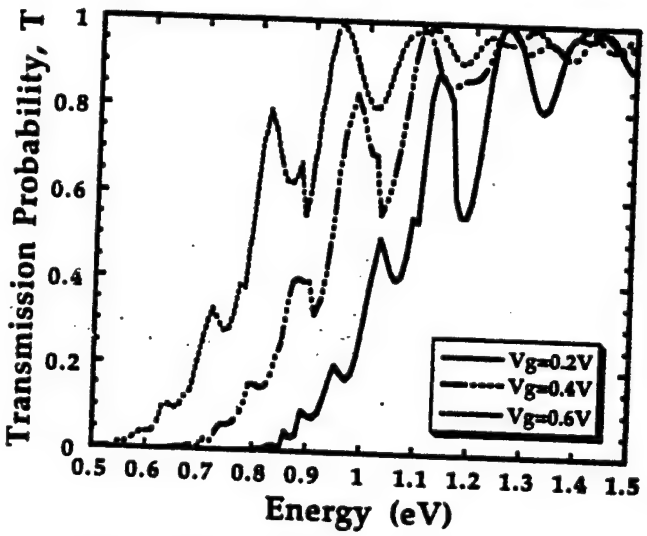


Figure 5.11. Transmission probability spectrum for electrons in the channel to transfer across the gate potential. The reference energy is the conduction band edge of the channel at the AlInAs spacer layer/GaInAs channel layer junction.

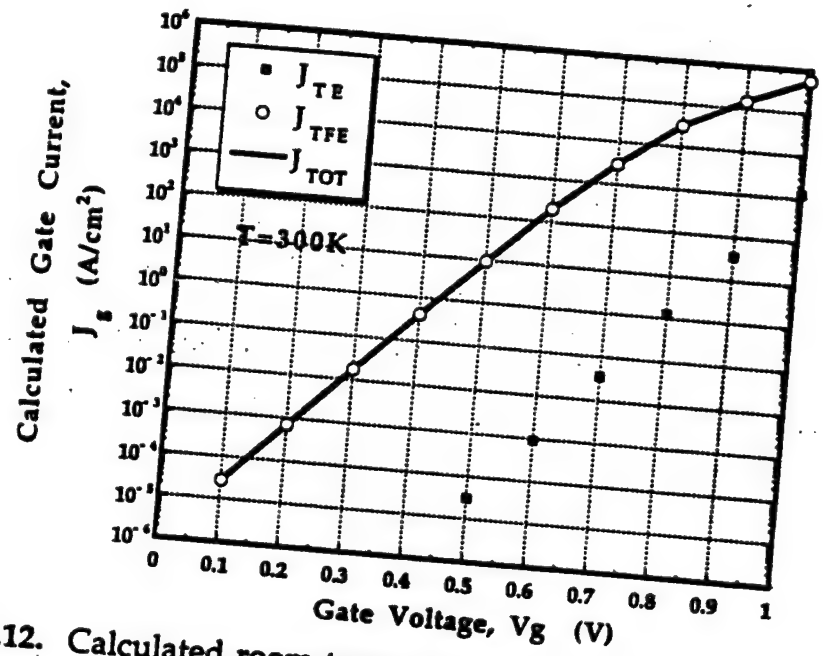


Figure 5.12. Calculated room temperature forward biased gate current density of the p$^+$-GaInAs/n-AlInAs/GaInAs JHEMT gate diode.

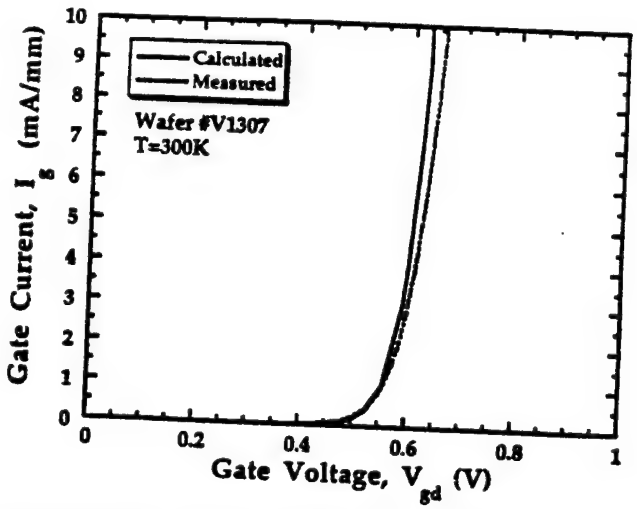


Figure 5.13. Comparison of the measured gate current and the calculated gate current.

gate current, resulting in Figure 5.13. The calculated gate current predicts that the measured turn-on voltage is $\approx 0.57eV$, significantly less than the peak barrier of 1.3eV. Further, the energy, where the transmission probability sharply rises, suggests that the turn-on voltage of p+-GaInAs/n-AlInAs/GaInAs JHEMT diode is determined by the bandgap of the p-type gate material and not the peak potential of the AlInAs barrier layer.

5.I.3 Threshold Voltage

The threshold voltage, of the device shown in Figure 5.5, is -0.8V. The reduced threshold voltage over the 0.2μm gatelength p+-AlInAs

JHEMT is directly attributed to a reduced barrier layer thickness (d_2), and high acceptor doping ($1x10^{20}$ cm^{-3}) in the gate layer.

5.I.3.1 Threshold Voltage Uniformity

As predicted in Chapter 2, the JHEMT exhibits high threshold voltage uniformity. Recall, the uniformity results from the fixed gate-to-channel separation determined by the accuracy of the layer thickness grown by Molecular Beam Epitaxy (M.B.E). Fifty devices were tested across a 1.5 x 1 $inch^2$ sample from wafer V1307. The threshold voltage was determined by linear extrapolation of the square root of the drain current. The average threshold voltage of the fifty devices was -.789V. Figure 5.14 contains a histogram showing the distribution of the threshold voltages. The standard deviation of threshold voltage of the 50 devices was 13.7mV. This standard deviation is comparable with the standard deviation of 1μm gatelength enhanced Schottky barrier HEMTs (using a depleted, p^+-GaAs surface layer) reported by Suzuki and coworkers[7] in 1986.

The threshold voltage of the JHEMT is established by the MBE (layer and doping) uniformity and the device aspect ratio (L_g/d_{p-2DEG}). The layer thickness variation is believed to be less than 2% across the 1.5 x 1 $inch^2$ sample. This alone only accounts for a 20mV span in the threshold voltage. In addition, the device aspect ratio of the JHEMT is only a function of the gatelength (since d_{p-2DEG} is fixed). Since the gatelength was fixed (0.2μm), the threshold voltage variations due to a deviating aspect ratio are believed to be negligible. Consequently, the threshold voltage

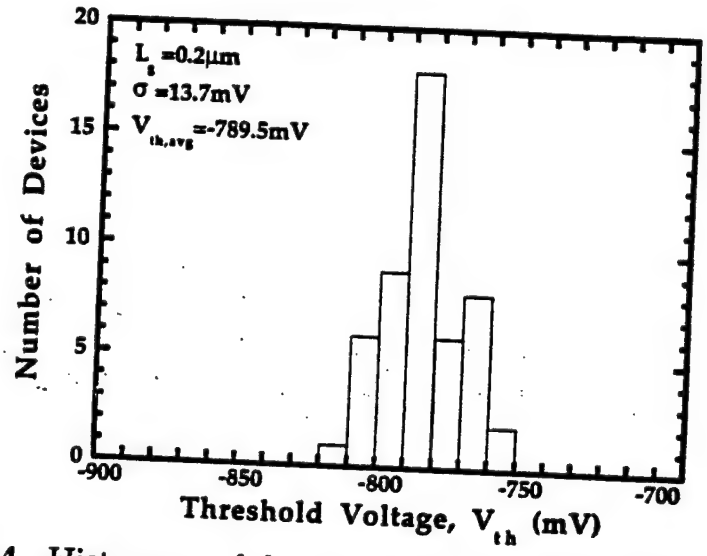


Figure 5.14. Histogram of the measured threshold voltage of 50 0.2μm gatelength JHEMTs from wafer #V1307. The devices were measured across a 1x1.5 in^2 wafer.

uniformity is limited by the doping uniformity across the sample. A 5% deviation in the donor layer doping would account for the 50mV span in threshold voltage observed in Figure 5.14.

5.I.3.2 Influence of Barrier Layer Thickness on threshold Voltage

Recall from chapter 2, the expression derived for the threshold voltage of the pseudo-planar-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT (equation [2.30]) may be written as:

$$V_{th} = \phi_{FC} - \frac{q \cdot N_d^{\,2} \cdot d_n^{\,2}}{2 \cdot N_A \cdot \varepsilon_1} - \frac{q \cdot (N_d \cdot d_n)}{\varepsilon_2} \cdot \left(d_2 + \frac{d_n}{2} \right) - E_{F,th} \qquad [5.3]$$

In the limit of high acceptor doping in the gate layer, equation [5.3] becomes

$$V_{th} \approx \phi_{FC} - \frac{q \cdot (N_d \cdot d_n)}{\varepsilon_2} \cdot \left(d_2 + \frac{d_n}{2} \right) - E_{F,th} \qquad [5.4]$$

where d_2 and d_n are the barrier layer thickness and the donor layer thickness, respectively. ϕ_{FC} is determined by the bandgap and doping of the gate material, and $E_{F,th}$ is influenced by the bandgap of the channel material. By design, d_2 is much greater than d_n and, therefore, d_2 most heavily influences the threshold voltage for a given donor layer doping.

5.I.4 RF Performance

5.I.4.1 Small Signal Performance

The microwave s-parameters (1-60GHz) were measured on-wafer using a Wiltron 360 Network Analyzer (NWA). The network analyzer was controlled by a host computer via the HP-IB control bus. The bias was provided from a HP 4145 parameter analyzer. In this section, the

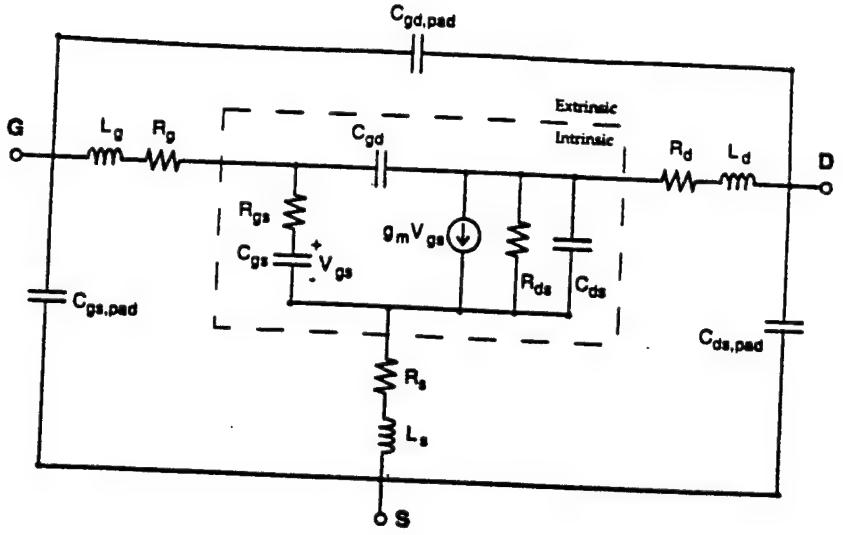


Figure 5.15. Equivalent circuit model of the JHEMT. The slashed-line separates the intrinsic FET parameters from the extrinsic parasitics. The model differs from the Schottky-barrier gate only by a modified extrinsic gate resistance, R_g.

small-signal circuit used to model the JHEMT is presented. Next, the device parasitics are examined, and the bias-dependent model parameters are reported. Finally, the current gain and power gain cut-off frequency performance is discussed.

Small-Signal Circuit Model

The full 17-element circuit model of the JHEMT including the parasitics is shown in Figure 5.15. The model consists of 8-intrinsic circuit elements and 9-extrinsic, parasitic elements. This model is identical to the Schottky HEMT model[8], if the expression for the gate resistance is

modified to include the ohmic contact resistance of the gate metal to the p^+-gate.

The extrinsic gate resistance, R_g, for the JHEMT including the gate contact resistance, may be written:

$$R_g = R_{g,feed} + R_{g,finger} + R_{g,contact} \qquad [5.5]$$

where

$R_{g,feed}$ is the gate metal feed resistance,

$R_{g,finger}$ is the metal finger resistance, and

$R_{g,contact}$ is the metal-semiconductor contact resistance.

Using the lumped element model derived in Appendix A, equation [5.5] may be written as:

$$R_g = R_{g,feed} + \left(\frac{R_{gee}}{W}\right) \cdot \frac{W}{3n^2} + \frac{\rho_c}{L_g \cdot W} \qquad [5.6]$$

If the third-term is removed, equation [5.6] reduces to the expression for gate resistance of a Schottky HEMT[9]. The gate resistance, R_g, can be calculated (if each component is accurately known) or estimated by the methods descibed in the next sub-section.

Extrinsic Device Parasitics

The nine extrinsic elements were obtained from the RF measurements of two-passive structures and one active device structure. Determination of the extrinsic parasitics from an active device structure has previously been reported elsewhere[10]. The three structures and the equivalent circuit model of each is shown in Figure 5.16. Using the

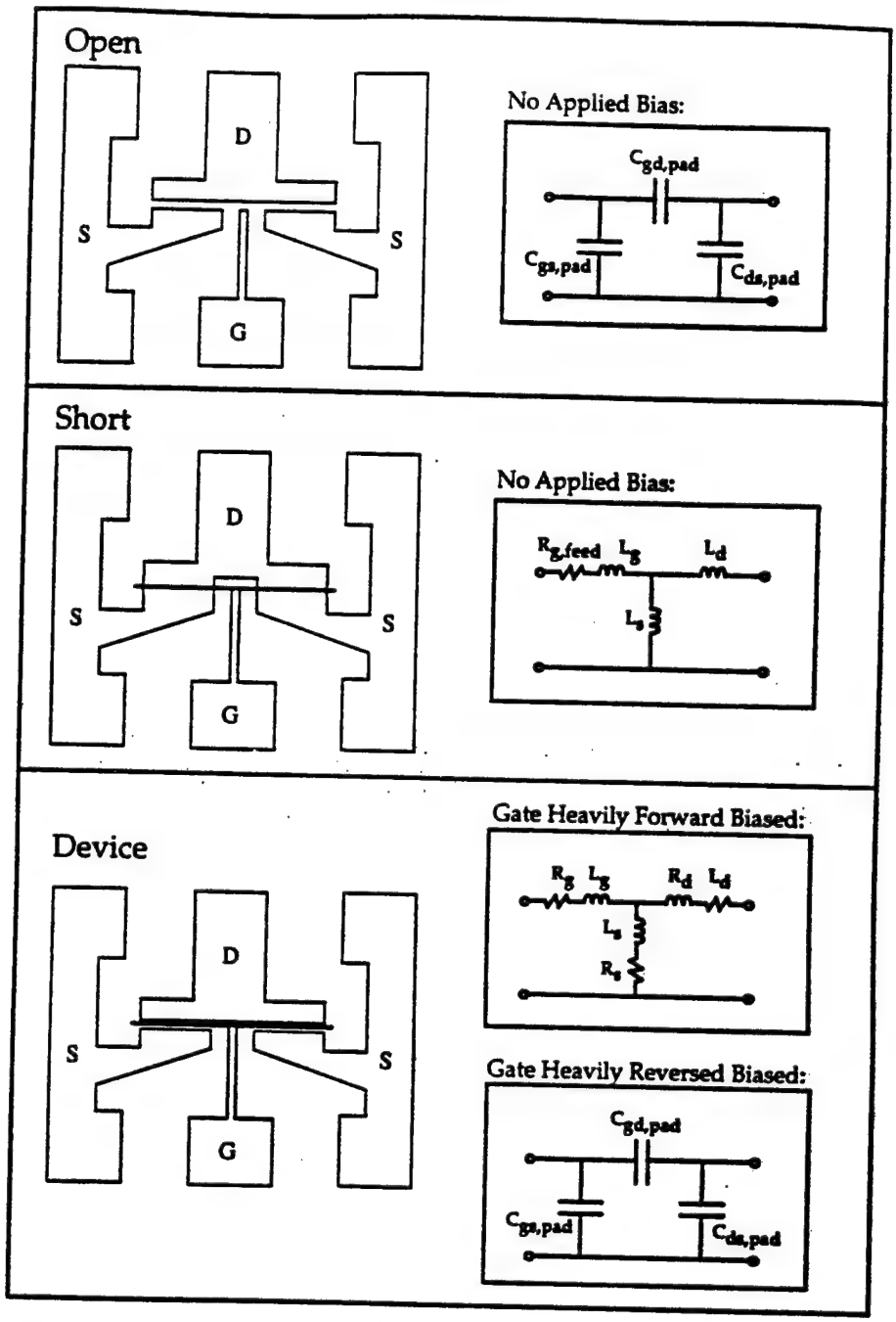


Figure 5.16. Three structure used to determine the extrinsic device parasitics. The equivalent circuits shown to the right of each structure indicate which elements are determined at the appropriate applied bias.

principles of a linear two-port networks, the circuit parameters are readily obtained in each structure.

First, the y-parameters of the open structure are measured to obtain the three pad capacitors ($C_{gs,pad}$,$C_{gd,pad}$, and $C_{ds,pad}$). Second, the z-parameters of the short structure are measured to obtain the three inductors (L_s,L_d, and L_g) and the gate feed resistance ($R_{g,feed}$). Next, the series resistors (R_s, R_d, and R_g) and series inductors (L_s,L_d, and L_g) may be extracted from the z-parameters of the active device under extreme forward-bias conditions. Finally, the device pad capacitors ($C_{gs,pad}$,$C_{gd,pad}$, and $C_{ds,pad}$) are obtained from the y-parameters of the device under heavy reverse-bias.

A summary of the device parasitics for the single doped p+-GaInAs/n-AlInAs/GaInAs JHEMT with a 100μm-wide gate finger is given in Figure 5.17. The lower values of capacitance for the open structure versus the device structure is clearly due to the intrinsic capacitance which present in the active device even under high reverse-bias. Similarly, the discrepancy in the source and drain inductance values is due to the metal proximity of the source and drain contacts in the two structures. The source and drain resistances were verified by TLM measurements. But, the gate resistance is believed to be over estimated due to the simplified assumptions made in determining the gate elements of the equivalent model (for the active device under conditions where the gate is heavily forward-bias) shown in Figure 5.16[11]. Nevertheless, the estimated value of gate resistance is used when extracting the intrinsic

Parameter	Measured Value	Test Structure
$C_{gs,pad}$	15 fF	open
	19.8 fF	device
$C_{gd,pad}$	7 fF	open
	9.3 fF	device
$C_{ds,pad}$	18 fF	open
	20.4 fF	device
L_s	7.8 pH	short
	5.2 pH	device
L_d	30.1 pH	short
	25.3 pH	device
L_g	29.3 pH	short
	30.4 pH	device
R_s	5.5 Ω	device
R_d	7.5 Ω	device
R_g	9.1 Ω	device
$R_{g,feed}$	1.4 Ω	short

Figure 5.17. The measured extrinsic device parasitics for the single-doped, p+-GaInAs/n-AlInAs/GaInAs JHEMT. The gatewidth of the structures is 100μm.

parameters, keeping in mind the possible discrepancy.

Bias-Dependent Model Parameters

The s-parameters of the single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT were measured as a function of gate voltage. In the device model in Figure 5.15, the nine extrinsic parasitics are assumed to be bias independent. Therefore, all the bias dependence is accomodated in the intrinsic model parameters.

In Figure 5.18, the intrinsic model parameters are plotted versus gate voltage, V_{gs}, at a constant drain voltage, V_{ds}, of +0.8V. The parameters are plotted in three figures. First, the transconductance, g_m, is plotted with the intrinsic gate-to-source capacitance, C_{gs}. The peak transconductance, $g_{m,max}$, is 750mS/mm and the maximum gate-to-source capacitance, $C_{gs,max}$, is 0.8pF/mm. Second, the three intrinsic device resistances are plotted. The large ratio of the intrinsic drain-to-source resistance, R_{ds}, to the intrinsic gate-to-source resistance, R_{gs}, is indicative of the high power gain (G_{max})[12] of this JHEMT. This ratio degrades as the device is operated in accumulation mode. Finally, the three intrinsic capacitances are plotted together. The total intrinsic gate capacitance ($C_g = C_{gs} + C_{gd}$) at -0.3V is 0.85pF/mm which is closer to the design rule of 1pF/mm[9] than the 0.6pF/mm of the p+-AlInAs gate JHEMT reported in Chapter 4. The higher intrinsic gate capacitance, C_g, results from the thinner barrier layer which reduces the gate-to-channel spacing.

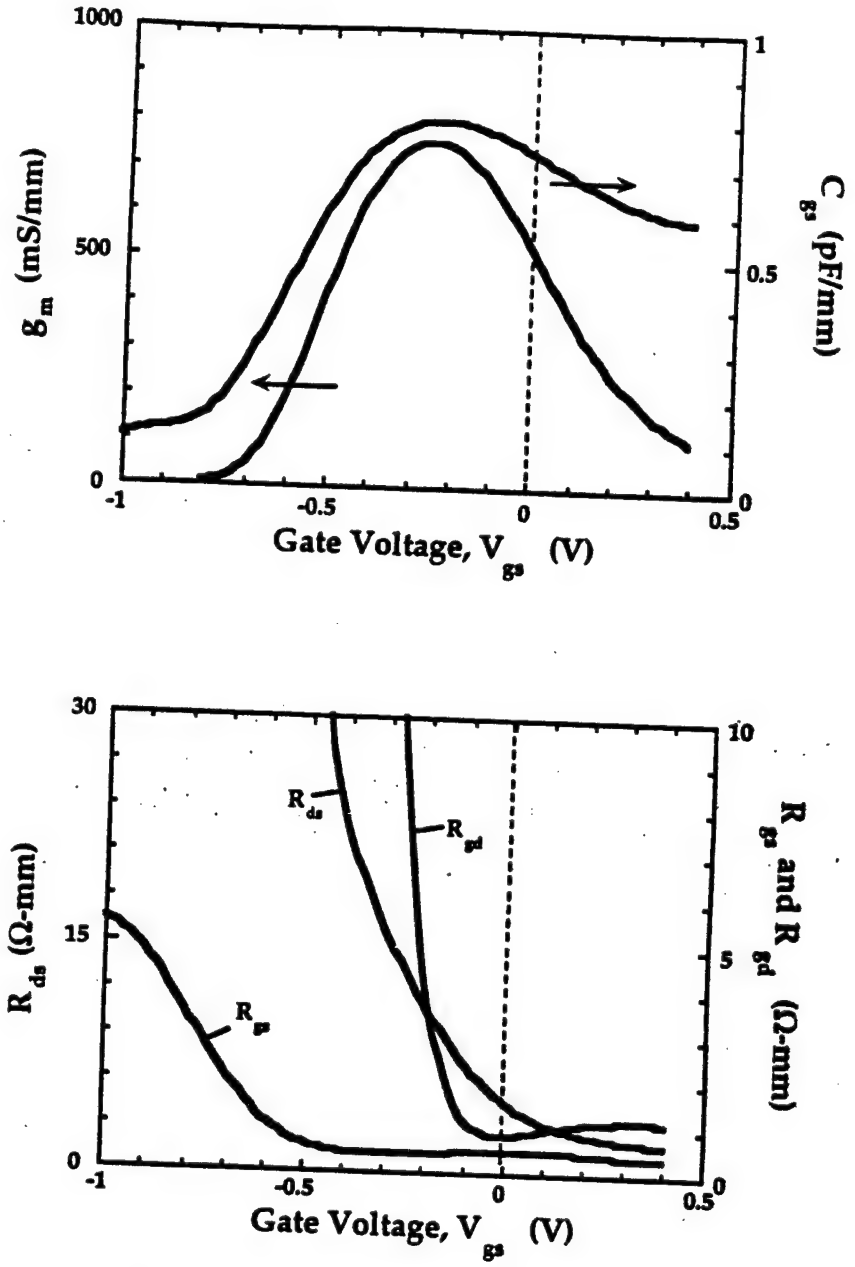


Figure 5.18. Intrinsic model parameters of the single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT (wafer #V1307) plotted versus gate voltage: g_m and C_{gs} (top), R_{ds},R_{gs}, and R_{gd} (bottom). The drain voltage, V_{ds}, is +0.8V.

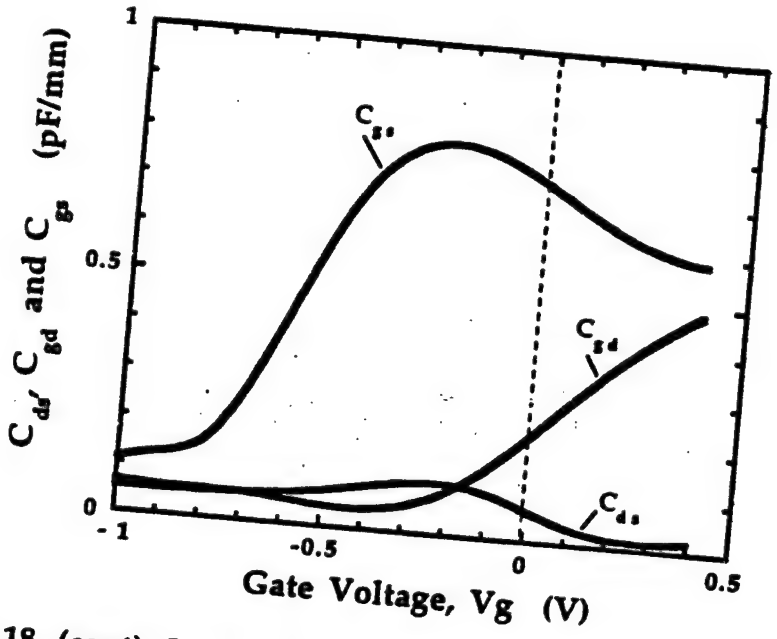


Figure 5.18. (cont) Intrinsic model parameters of the single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT (wafer #V1307) plotted versus gate voltage: C_{ds},C_{gd},C_{ds}. The drain voltage, V_{ds}, is +0.8V.

Current Gain and Power Gain

The intrinsic unity current gain cut-off frequency[13] $\left(f_{\tau,intrinsic}\right)$ of a HEMT which is indicative of the intrinsic device speed is defined by:

$$f_{\tau,intrinsic} = \frac{g_m}{2\pi \cdot C_{gs}} = \frac{v_{sat}}{2\pi \cdot L_g} \qquad [5.7]$$

where v_{sat} is the saturation velocity and L_g is the effective gatelength. To determine $f_{\tau,intrinsic}$, the intrinsic[14] short circuit current gain (h_{21}) may be extrapolated 20dB/dec to unity gain. Alternatively, the value may be calculated from the intrinsic device parameters once they are known. The measured gate dependence of the intrinsic unity current gain cut-off frequency can be observed in the plot of g_m and C_{gs} versus V_{gs} (see Figure 5.18). However, it is the extrinsic unity current gain cut-off frequency $\left(f_{\tau,extrinsic}\right)$ which reflects the terminal speed of the device including the parasitic transit delays. The extrinsic unity current gain cut-off frequency is readily converted to the total transit delay through the device

$$\tau_{total} = \frac{1}{2\pi \cdot f_{\tau,extrinsic}} = \tau_{intrinsic} + \tau_{parasitic} \qquad [5.8]$$

which may be expanded[15]:

$$\tau_{total} = \frac{(C_{gs} + C_{gd})}{g_{mo}} + \frac{(C_{gs} + C_{gd}) \cdot (R_s + R_d)}{g_{mo} \cdot R_{ds}} + C_{gd} \cdot (R_s + R_d) \qquad [5.9]$$

The extrinsic unity current gain cut-off frequency is determined either by calculating the delays in equation [5.9] or by extrapolating 20dB/dec from the extrinsic short-circuit current gain (h_{21}) to unity gain. Finally, the unity power gain cut-off frequency (f_{max}) can be approximated by[16]:

$$f_{max} = \frac{f_\tau}{2 \cdot \sqrt{\left(\frac{R_g + R_{gs} + R_s}{R_{ds}} + 2\pi \cdot f_\tau \cdot R_g \cdot C_{gd} \right)}} \qquad [5.10]$$

where the negative feedback of the source inductance (L_s) is neglected. To achieve a high f_{max}, a high extrinsic unity current gain cut-off frequency is needed along with a high input-to-output resistance ratio. Therefore, the gate and source resistance must be minimized. The low gate-to-drain capacitance, C_{gd}, obtained by modulation doping (e.g. see C_{gd} of the JHEMT, Figure 5.18) minimizes the the input losses due to feedback.

A plot of gain versus frequency (1-60GHz) at V_{ds} = +0.8V, and V_{gs} = -0.3V is given in Figure 5.19. From the short-circuit current gain, the extrinsic f_τ of the 0.2μm gatelength, single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT is 105GHz. From the maximum stable gain (MSG) and the unilateral power gain (U), the unity power gain cut-off frequency (f_{max}) is 170GHz.

In Figure 5.20, the extrinsic unity gain cut-off frequencies, f_τ and f_{max}, of the 0.2μm gatelength single-doped p+-GaInAs gate JHEMT are plotted versus gate voltage (top) and drain voltage (bottom). The f_τ inboth plots was measured from the short-circuit current gain. The f_{max} plotted versus gate voltage was calculated using equation [5.10] along with the parameters shown in Figure 5.18. The f_{max} plotted versus drain voltage was extrapolated from the maximum available power gain (MAG) and is compared to f_{max} calculated from equation [5.10]. The f_τ and f_{max}

trends are very similar to bias dependent measurements of Schottky-gate HEMTs reported elsewhere[8].

The peak f_τ is 105GHz at V_{ds}=+0.8V and the roll-off at higher drain voltages is due to the decrease in output resistance, R_{ds}, which increases the transit delay through the device as seen in equation [5.9]. At V_{ds}=2V, the f_τ has dropped to approximately 80GHz. From both the measured maximum available gain and the model calculation, the f_{max} is over 200GHz at V_{ds}=1V. To this author's knowledge, this is the highest f_{max} ever reported for a junction gate-barrier FET (JFET).

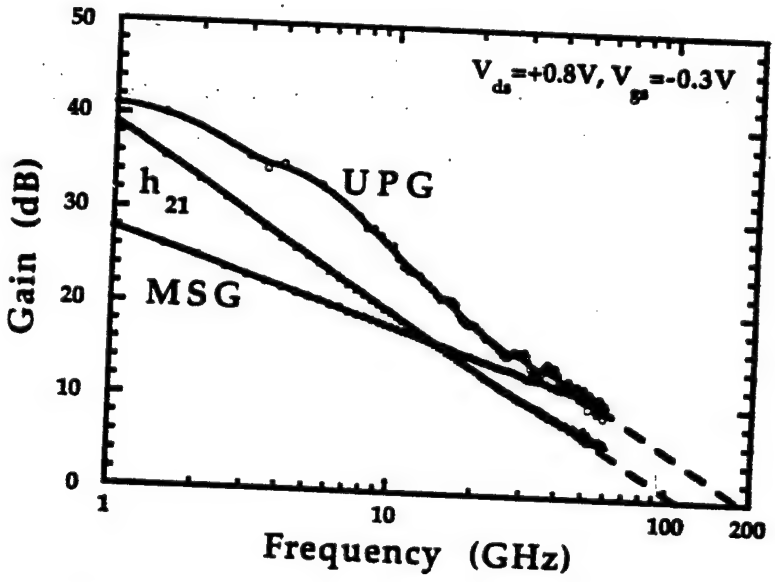


Figure 5.19. Gain versus frequency of the single-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT. The drain voltage is +0.8V, and the gate voltage is -0.3V. The extrinsic f_τ and f_{max} are 105GHz and 170GHz, respectively.

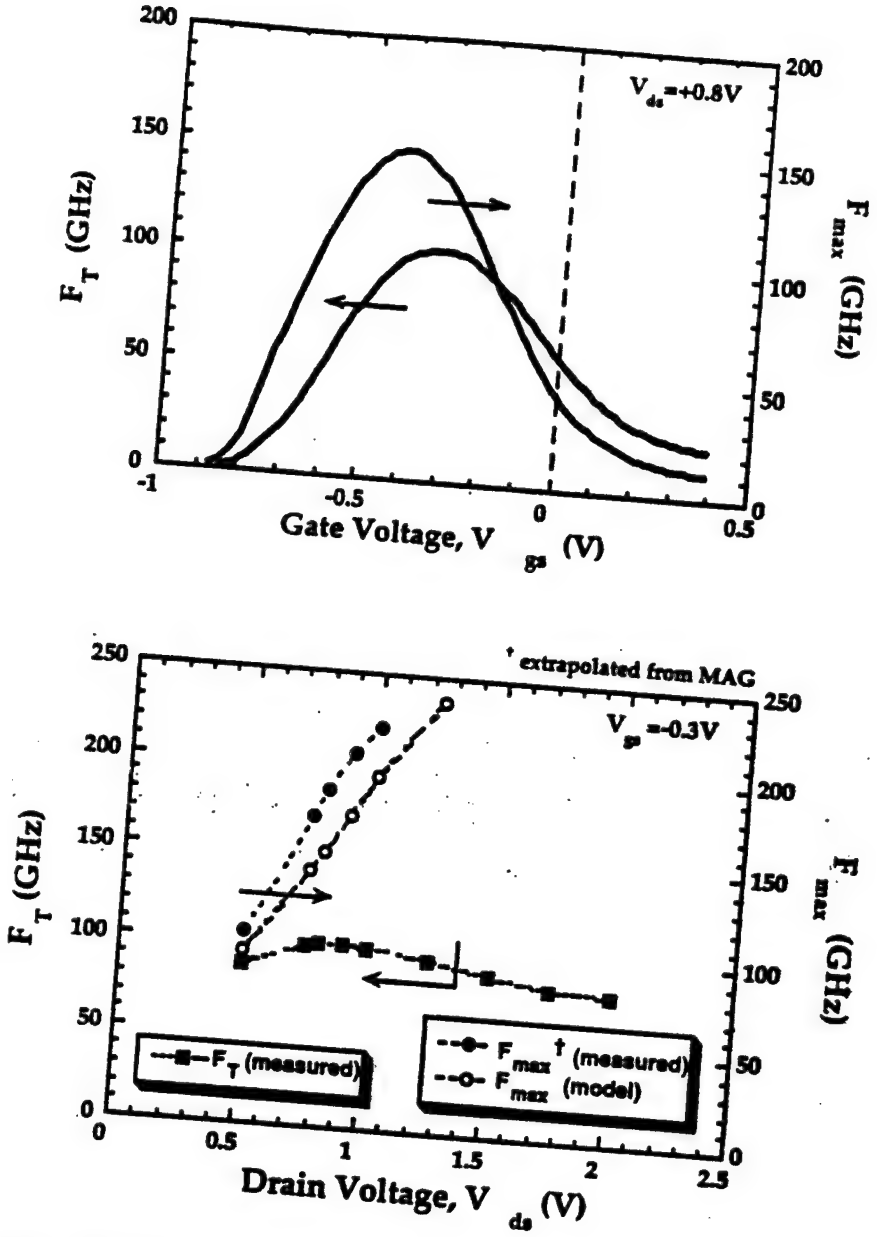


Figure 5.20. Bias dependence of unity gain cut-off frequencies. In the top figure, the f_t was measured and the f_{max} is calculated from equation [5.11] using the device parameters in Figures 5.19 and 5.20. In the bottom figure, both f_t and f_{max} was measured and the measured f_{max} is compared to the f_{max} calculated from equation [5.11].

5.I.4.2 Noise-Parameter Performance

Several authors[17,18,19] have published noise models which predict the minimum noise figure (F_{min}) versus frequency for a field effect transistor or HEMT. Fukui's semi-empirical model[18] expressed the F_{min} by:

$$F_{min} = 1 + K_f \cdot \frac{f}{f_\tau} \cdot \sqrt{g_m \cdot (R_g + R_s)} \qquad [5.11]$$

where K_f is the frequency independent Fukui fitting factor, and the other terms were all defined in the model presented in Figure 5.15. Equation [5.11] predicts F_{min} at any frequency once the fitting factor is determined from measurements at one particular frequency.

Pospieszalski's model[19] assumed the gate and drain noise sources were of thermal origin only. The simplified intrinsic model (with appropriate noise sources) representing the noise equivalent circuit is shown in Figure 5.21. The intrinsic feedback branch was moved into the extrinsic part of the circuit where all the extrinsic noise sources (due to R_g,R_s,R_d, and R_{gd}) can be represented by each resistance at the ambient temperature (T_a). The noise sources of the intrinsic device consist of the gate-to-source resistance at T_a and the output conductance, G_{ds}, at a particular drain temperature, T_d. In this model, the drain temperature serves as the fitting factor. The expression obtained for F_{min} is:

$$F_{min} = 1 + \frac{\sqrt{T_a \cdot T_d}}{T_o} \cdot \left(\frac{f}{f_\tau}\right) \cdot \sqrt{4 \cdot G_{ds} \cdot R_{gs}} \qquad [5.12]$$

where T_o is the standard noise temperature (290K). Remarkably, equation [5.12] has the same frequency dependence as equation [5.11]. Equation

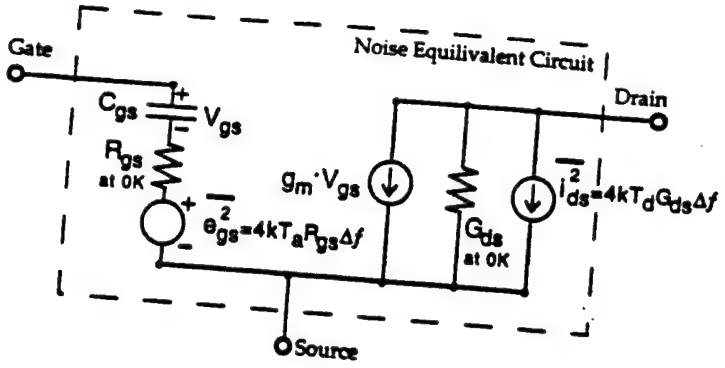


Figure 5.21. Noise equivalent circuit of the intrinsic device model. For convenience the feedback capacitance has been moved to the extrinsic circuit (after Pospieszalski[19]).

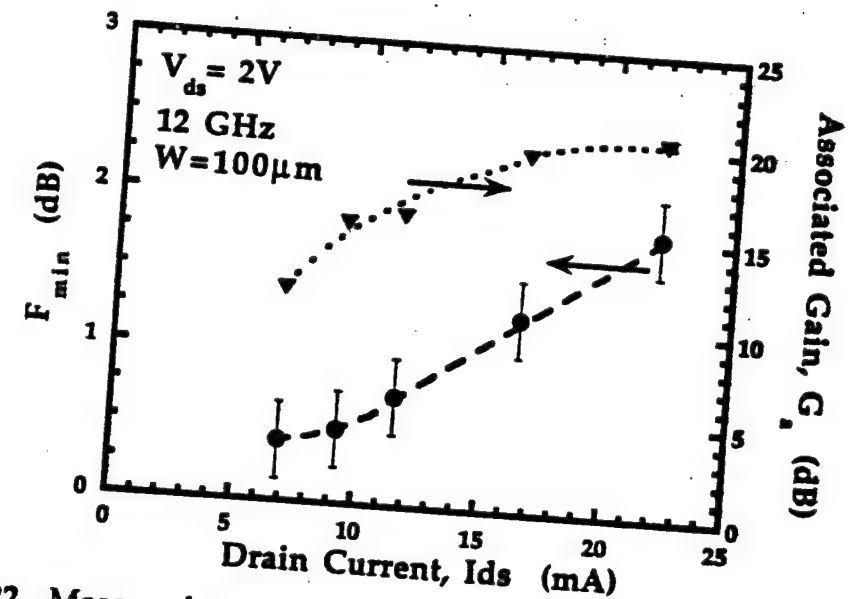


Figure 5.22. Measured minimum noise figure (F_{min}) and associated gain (G_a) versus drain current (I_{ds}) of the 100μm-wide p^+-GaInAs gate JHEMT.

[5.12] may be expressed in terms of f_{max} by substituting equation [5.10] and considering only the model parameters shown in Figure 5.21. Equation [5.12] becomes:

$$F_{min} = 1 + \frac{\sqrt{T_a \cdot T_d}}{T_o} \cdot \left(\frac{f}{f_{max}} \right) \qquad [5.13]$$

Qualitatively, the common theme expressed in equations [5.11] thru [5.13], is the need for low parasitics (e.g. R_s, R_g, R_d, C_{gd}, and G_{ds}) and high cut-off frequencies, f_τ and f_{max}. The high f_τ (100GHz) and f_{max} (>200GHz) and low parasitics of the 0.2μm gatelength single-doped, p+-GaInAs gate JHEMT prompted the measurement of the noise-parameters.

The noise parameters were measured on-wafer at 12 GHz using an automated tuning network (ATN) system equipped with a HP 8510C Network Analyzer, Series Synthesized Sweeper, Noise Figure Meter, and Noise Figure Test Set. The device bias was supplied by a HP4145 Parameter Analyzer. The minimum noise figure (F_{min}) and associated gain (G_a) of the 100μm wide, p+-GaInAs gate JHEMT were measured versus drain current at 6 and 12GHz with V_{ds}=+2V, and the F_{min} and G_a at 12 GHz versus drain current are shown in Figure 5.22. At 6 GHz and I_{ds}=9mA, the F_{min} and G_a are 0.25dB[20] and 18.5dB, respectively. At 12 GHz with I_{ds}=9mA, state-of-the-art F_{min} (0.45dB) and G_a (14.5dB) are obtained. The noise performance and gain of the p+-GaInAs gate JHEMT are compared with GaAs- and InP-based Schottky-gate HEMT technologies in Figure 5.23.

For completeness, the noise performance of the 0.2μm gatelength, p+-GaInAs gate JHEMT is compared to the noise performance of the 0.5μm gatelength, p+-GaAs gate JHEMT reported by Ohata and coworkers[21] (see Figure 5.24).

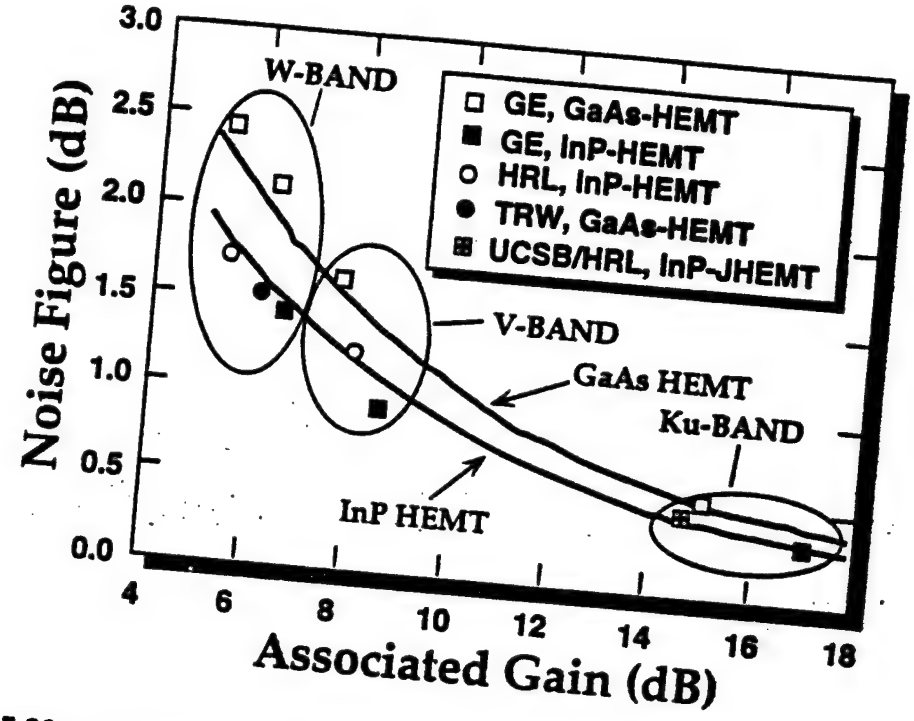


Figure 5.23. Comparison of the measured noise performance of the p+-GaInAs gate JHEMT to the noise figure of state-of-the-art low-noise HEMTs.

Reference	JHEMT	Lg	Rs	Ids	Fmin (Ga) at 12GHz
Ohata [21]	GaAs	0.5 μm	0.7Ω-mm	10mA	1.2dB (11.7dB)
this work	InP	0.2μm	0.55Ω-mm	9mA	0.45dB (14.5dB)

Figure 5.24. Comparison of the noise performance of GaAs- and InP-based JHEMTs.

II. Double-Doped p+-GaInAs/n-AlInAs/ GaInAs JHEMTs

In the second half of the chapter, the performance of the double-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT is presented. First the layer design of the double-doped p+-GaInAs/n-AlInAs/GaInAs wafer is discussed. The material profile of the wafer used to fabricate the double-doped, p+-GaInAs gate JHEMTs is also provided. Next, the dc characteristics of the 0.15μm, 0.33μm ,0.47μm gatelength p+-GaInAs/n-AlInAs/GaInAs JHEMTs are presented. Also, the gate resistance for various gatelengths and doping in the gate layer is summarized Finally, the microwave performance of the double-doped JHEMT is examined, including the gatelength dependence on small-signal model parameters.

5.II.1 Layer Structure

As mention in Chapter 1, the double-doped HEMT structure consists of donor region impurities both above and below the channel. The additional donor layer below the channel requires the channel thickness to be reduced in order to minimize the distance between the gate and the centroid of the additional channel electrons. With this modification in mind, the layer structure of the double-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT is presented in Figure 5.25. The bottom donor layer consists of a planar sheet ($1.5x10^{12} cm^{-2}$) Si-impurities. The planar doping is placed 50Å away from the channel as shown. The channel thickness is reduced to 150Å. Four modifications were made to the layers above the channel shown in Figure 5.2. First, the spacer layer

200Å	Gate	GaInAs	P=3x10^{19} cm^{-3}
120Å	Barrier	AlInAs	
30Å	Donor	AlInAs	N=2x10^{19} cm^{-3}
25Å	Spacer	AlInAs	
150Å	Channel	GaInAs	
50Å	Spacer	AlInAs	
2500Å	Buffer	AlInAs	n=1.5x10^{12} cm^{-2}
	Substrate	InP	

Figure 5.25. Layer structure of the Double-Doped p^{+}-GaInAs/n-AlInAs/GaInAs JHEMT.

thickness was increased with the intention of increasing the channel mobility as suggested from Figure 5.3. Second, the thickness of the donor layer was reduced and the doping was increased in order to reduce the gate-to-channel distance. However, the doping-thickness product remain a constant ($6x10^{12}cm^{-2}$)[22]. Next, the barrier layer thickness was increased in order to transfer more of the charge to the channel. Finally, the doping in the gate was reduced to p=$3x10^{19}cm^{-3}$ to observe the doping dependence on gate resistance.

The material profile of the double-doped-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT is shown in Figure 5.26. The device structure was grown by *T. Liu* of Hughes Research Laboratories. The minimum sheet resistance obtainable in the access regions of the double-doped JHEMT (V1401) is 240Ω/sq compared to 290Ω/sq for the single-doped JHEMT (V1307). As expected, the carrier concentration is higher in the double-doped JHEMT ($3.2x10^{12} cm^{-2}$), but the mobility is slightly lower ($7800 \frac{cm^2}{V \cdot s}$).

5.II.2 Device Layout

The width of the double-doped p+-GaInAs/n-AlInAs/GaInAs JHEMTs studied was 100μm. The purpose of this wafer was to compare devices with different gatelengths. Thus, three different gatelengths were fabricated on the same wafer to compare performance. The three gatelengths chosen were 0.15μm, 0.33μm, and 0.48μm. The SEM inspection of each gatelength (prior to gate metal deposition) is shown in Figure 5.27. The device geometry was relaxed in the double-doped JHEMT in order to accommodate the larger gatelengths. The source-drain spacing of the devices with different gatelengths is 3μm compared to 2μm for the devices reported in the last chapter. In addition to the multi-gatelength 3μm devices, 0.15μm gatelength devices with 2μm source-drain spacing were also fabricated on the same wafer. In all devices reported in this chapter, the gate-source spacing is 0.7μm compared to 0.5μm for the single-doped JHEMTs reported earlier.

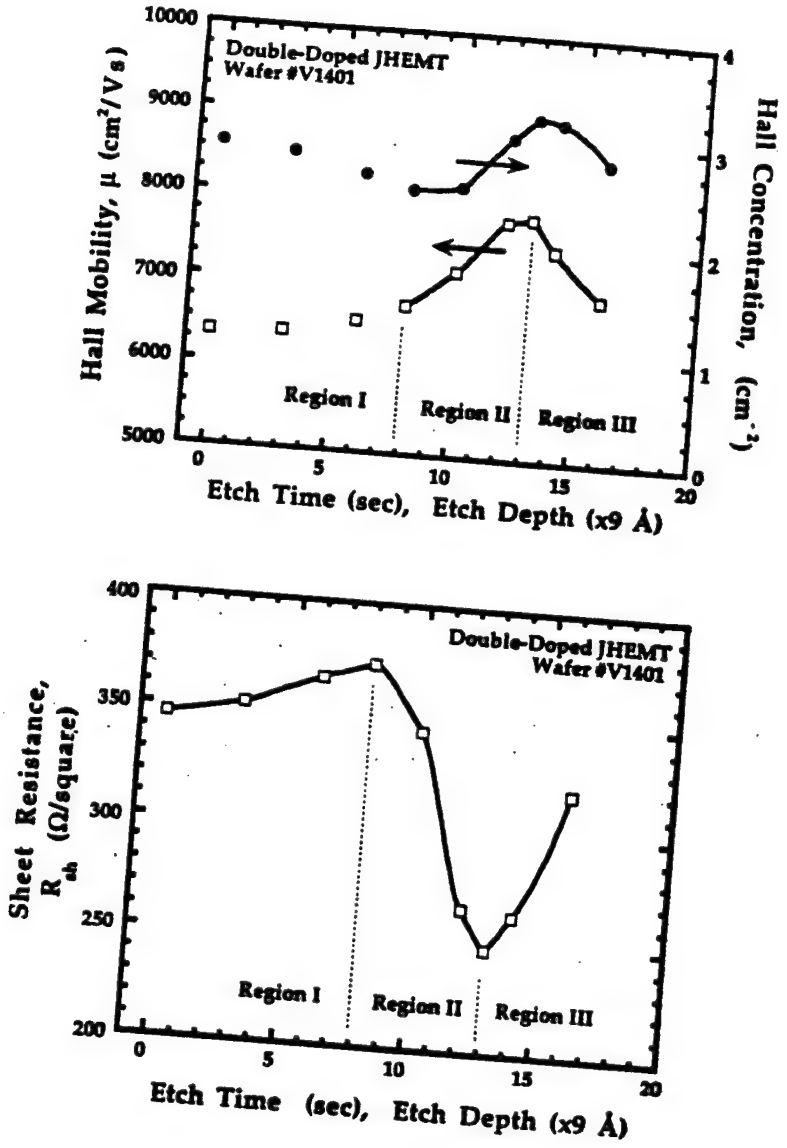


Figure 5.26. Material profile for the double-doped, p⁺-GaInAs/n-AlInAs/GaInAs JHEMT (wafer #V1401). The electron sheet resistance (top), and the electron mobility and sheet concentration (bottom) are shown.

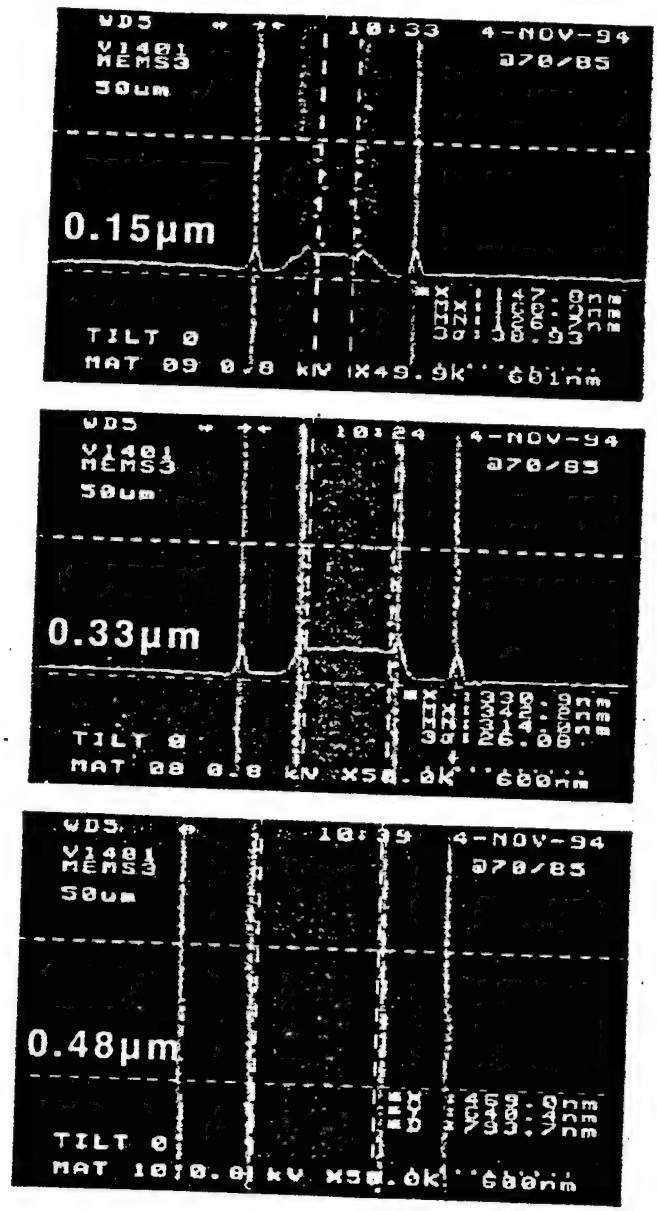


Figure 5.27. Low voltage SEM inspection of the three devices with different gate openings. These micrographs were taken prior to metal deposition.

5.II.3 DC Characteristics

A plot of g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V) for 2μm source-drain spacing, double-doped JHEMT with 0.15μm gatelength is shown in Figure 5.28. The full channel current and maximum dc transconductance of the 100μm device is 550mA/mm and 550mS/mm, respectively. Compared to the single-doped JHEMT (Lg=0.2μm) in Figure 5.5, the double-doped exhibits 20% higher current density (due to higher carrier concentration) and a 5% percent increase in dc transconductance (due to slightly lower source resistance).

Plots of g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V) for the 3μm source-drain spacing, double-doped JHEMTs (with 0.15μm, 0.33μm, and 0.48μm gatelengths) are shown in Figure 5.29. Similar transconductance and full channel current were obtained from the three devices with different gatelengths. The two subtle changes observed for the devices with different gatelengths were (i) a threshold voltage shift, and subsequently (ii) a shift in the peak transconductance. A plot of $\sqrt{I_{ds}}$ versus V_{gs} (which is used to determine the threshold voltage) is shown in Figure 5.30. A threshold voltage shift of 200mV is observed from the 0.48μm gatelength to the 0.15μm gatelength device. However, the threshold voltage shift is only 40mV when the gatelength changes from 0.48μm to 0.33μm. Therefore, the observed shift is not linear with gatelength. Further this shift in threshold voltage shifts the peak transconductance toward a more positive gate voltage for a larger gatelength. A summary of the threshold voltage, peak transconductance for the three gatelengths is given in Figure

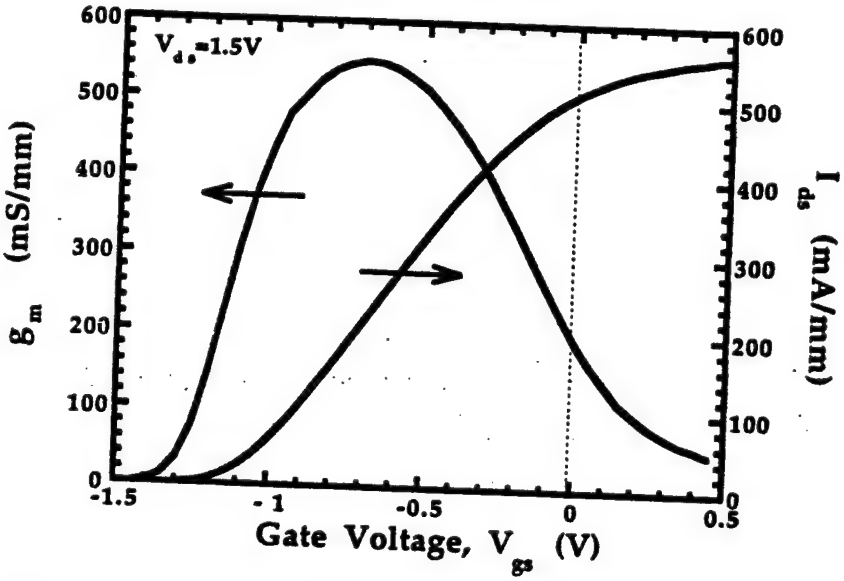


Figure 5.28. g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V) for 2μm source-drain spacing, double-doped JHEMT with 0.15μm gatelength.

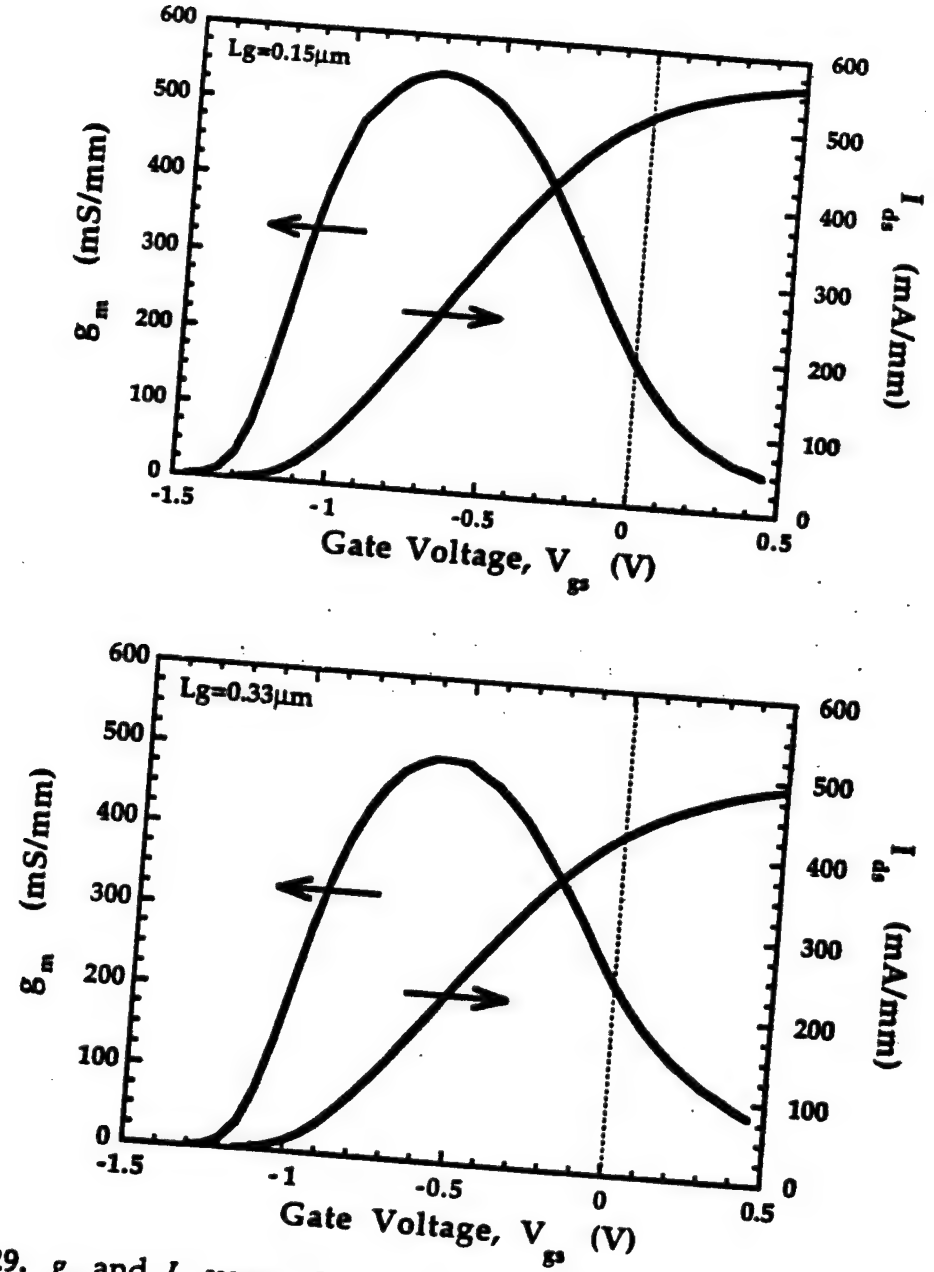


Figure 5.29. g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V, L_{sd}=3μm) for double-doped JHEMTs with 0.15μm (top) and 0.33μm (bottom) gatelengths.

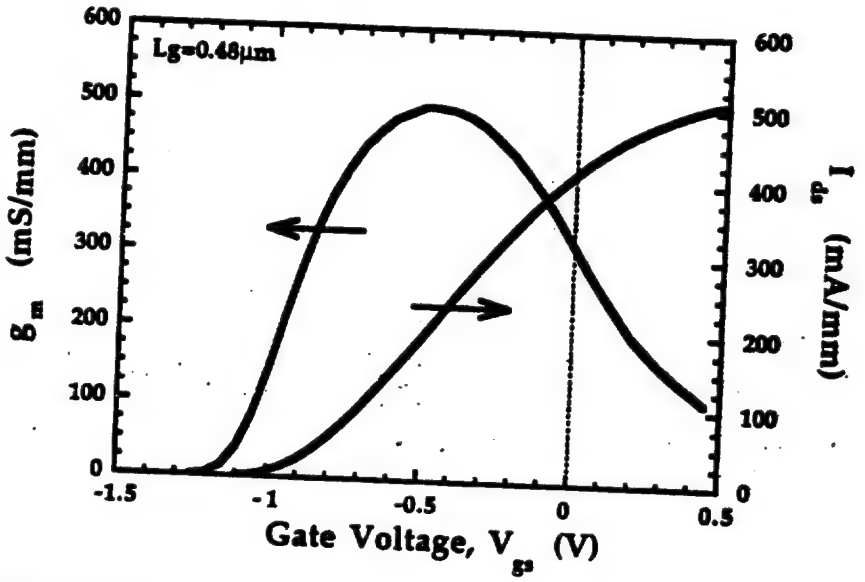


Figure 5.29. (cont) g_m and I_{ds} versus V_{gs} (V_{ds}=1.5V, L_{sd}=3μm) for the double-doped JHEMT with 0.48μm gatelength.

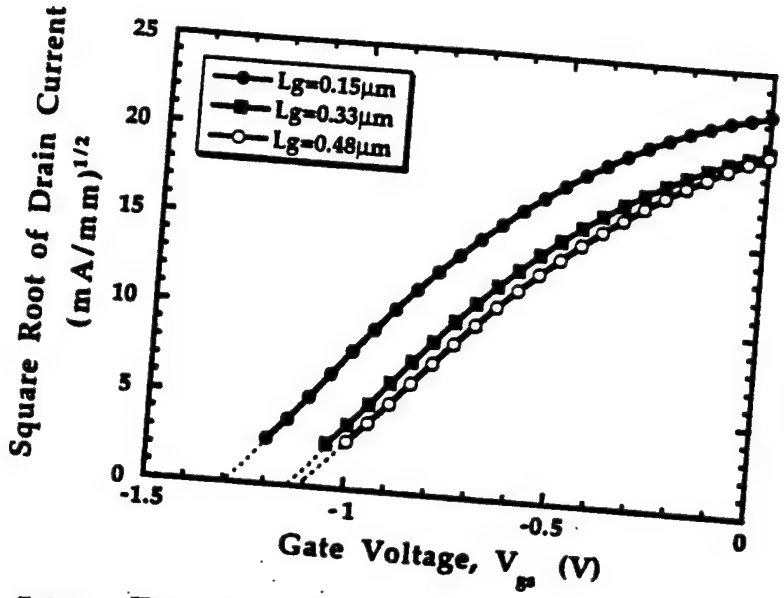


Figure 5.30. $\sqrt{I_{ds}}$ versus V_{gs} (V_{ds}=1.5V) for the 3μm source-to-drain spacing, double-doped JHEMTs. The threshold shift is attributed to the varying aspect ratio.

L_g (μm)	V_{th} (V)	V_g at $g_{m,peak}$ (V)
0.15	-1.3	-0.7
0.33	-1.14	-0.5
0.48	-1.1	-0.45

Figure 5.31. Threshold voltage and the gate voltage at peak transconductance for the 0.15μm, 0.33μm, and 0.48μm gatelength JHEMTs. The threshold voltage shift results in the peak transconductance shift to more positive values

5.31. The shift of threshold voltage and subsequently the peak transconductance is attributed to the degrading aspect ratio for short gatelengths.

Finally, it is appropriate to note that the threshold voltage has changed from -0.8V to -1.3V (depending on gatelength) from the single-doped structure to the double-doped structure. The additional negative voltage which must be applied to the gate to meet the threshold condition is accounted for by two separate factors. Not only do the additional impurities (placed below the channel) increase the threshold voltage, but also the lower doping in the gate region increases the potential drop (in the gate region) required to meet the flat band condition. This increase in potential drop across the gate is manifested by the second term in equation [5.3].

5.II.4 RF Performance

In this section, the gate resistance of the 0.15μm, 0.33μm, and 0.48μm gatelength, double-doped JHEMTs is compared to the gate resistance of the 0.2μm gatelength JHEMTs presented in Chapter 5. Afterwards, the other extrinsic parasitics are discussed. Then, the bias-dependent model parameters are presented for the 0.15μm gatelength device with source-to-drain spacing of 2μm. Finally, the bias dependent current gain and power gain cut-off frequencies are discussed.

Gate Resistance

Recall, the doping in the gate layer of the single-doped JHEMT is $1x10^{20}cm^{-3}$. The gate layer doping in the double-doped JHEMT is reduced to $3x10^{19}cm^{-3}$ in order to study variations in the total gate resistance. A summary of the gate resistance versus gate layer doping and gatelength is given in Figure 5.32. As expected, the gate resistance rises sharply when the doping in the gate layer is decreased. Consistent, with the model presented in Chapter 2, the gate resistance rises when the gatelength is reduced (for a constant gatewidth).

Wafer	L_g (μm)	W_g (μm)	N_A (cm^{-3})	R_g (Ω)
V1307	0.2	100	$1x10^{20}$	9.1
V1401	0.15	100	$3x10^{19}$	16
V1401	0.33	100	$3x10^{19}$	10
V1401	0.48	100	$3x10^{19}$	7.5

Figure 5.32. Table summary of the total extrinsic gate resistance for various gatelengths and gate layer doping.

Other Extrinsic Parasitics

The 100μm-wide device layout of the double-doped JHEMT was similar to the layout of the single-doped JHEMTs reported in the last chapter. The two differences were the source-drain spacing and the varying gatelength as discussed in section 5.II.2. The nine extrinsic parasitics were re-measured and the 3 pad capacitances and 3 inductances

were similar to the values reported in Figure 5.17. However, the three extrinsic resistances were different. The extrinsic gate resistance increased as discussed in the previous section and the values are summarized in Figure 5.32.

The measured extrinsic source resistance for the 0.15μm, 0.33μm and 0.48μm gatelength devices is 5.3Ω, 5.5Ω, and 5.3Ω, respectively. The measured extrinsic drain resistance for the 0.15μm (L_{sd}=2μm), 0.15μm (L_{sd}=3μm), 0.33μm and 0.48μm gatelength devices is 7.5Ω, 10.6Ω, 10.0Ω, and 9.3Ω, respectively. The lower resistance for the longer gatelength is due to the shorter gate-to-drain separation.

Model Parameters and Unity Gain Cut-Off Frequencies

The s-parameters of the double-doped p+-GaInAs/n-AlInAs/GaInAs JHEMT were measured as a function of drain voltage, V_{ds}. The shorter gatelength (0.15μm) leads to a higher extrinsic f_τ of 118 GHz as shown in Figure 5.33. The intrinsic transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}) are plotted versus drain voltage in Figure 5.34, from which the calculated intrinsic f_τ using the saturated velocity model (SVM) is 170GHz.

The higher gate resistance (due to lower doping in the gate layer and shorter gatelength) translates into a lower f_{max} than the single-doped JHEMT. The calculated f_{max} from equation [5.11] using the measured small signal parameters is plotted in Figure 5.35. Also, the drain dependence of the measured extrinsic f_τ and the output conductance, G_{ds}, are also plotted. The trends of the four model parameters and the two cut-

off frequencies are consistent with the trends discussed by Hughes and Tasker[8] for Schottky HEMTs. The interested reader is directed to Appendix F, where the bias dependent model parameters of the 3μm (L_{sd}) devices with different gatelengths (0.15, 0.33, and 0.48μm) are presented.

To observe the gatelength dependence of f_τ and f_{max}, the measured extrinsic f_τ and the calculated f_{max} are plotted in Figure 5.36 for different gatelengths. Clearly, the higher f_τ for the 2μm (L_{sd}) device over the 3μm (L_{sd}) device is due to the lower parasitic drain delay for the shorter channel. The decrease in f_τ as the gatelength increases is due to the higher gate capacitance. Since f_{max} is proportional to f_τ, the general trend

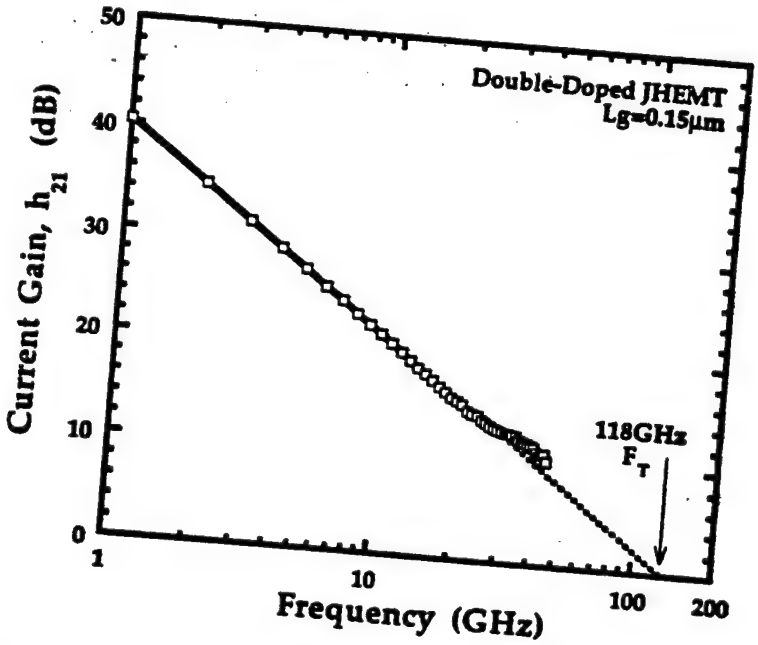


Figure 5.33. Short-circuit current gain versus frequency for the 0.15μm gatelength double-doped JHEMT with device width of 100μm.

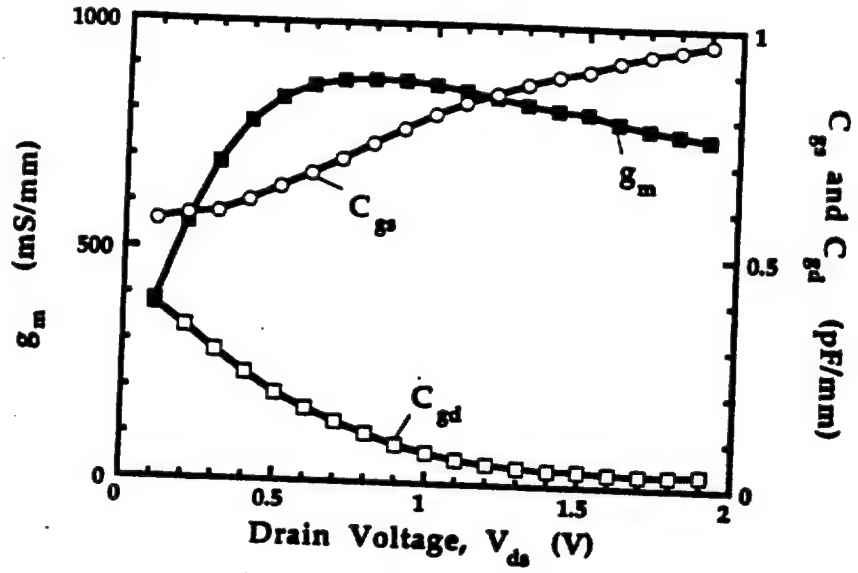


Figure 5.34. Small signal transconductance and gate capacitance versus drain voltage for the 0.15µm gatelength, double-doped JHEMT with source-to-drain spacing of 2µm.

should be maintained. At low voltages, the high output conductance and high gate resistance reduce the f_{max}/f_t ratio. At higher drain voltages, the output conductance drops, which increases the input-to-output resistance ratio. Consequently, the ratio of f_{max}/f_t rises as seen in Figure 5.36. The higher f_{max}/f_t obtained for the longer gatelength device is due to the lower gate resistance as the gate area increases, and increased isolation between the gate and drain (i.e. lower C_{gd}/C_{gs} ratio).

In summary, the gate resistance dominates the input resistance in the 0.15µm double-doped JHEMTs reported in this section. The higher

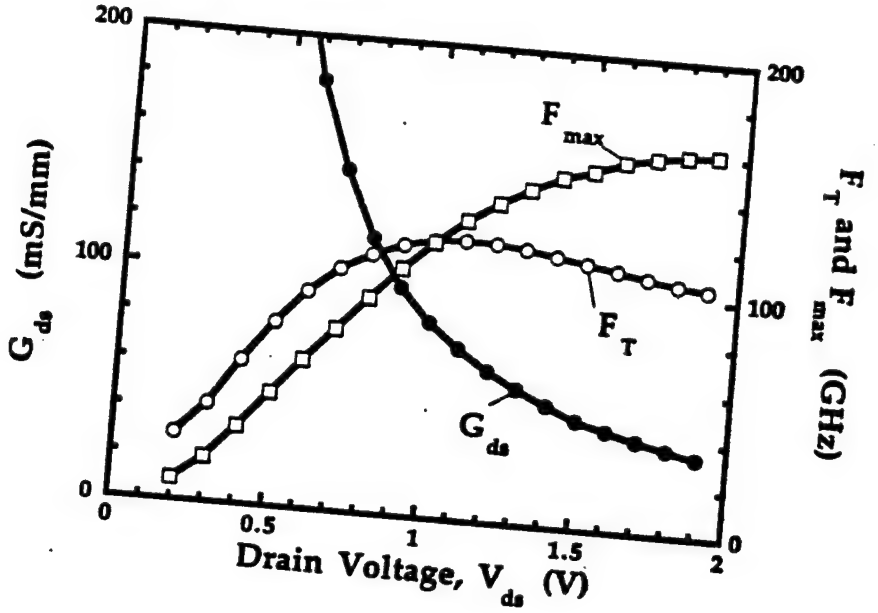


Figure 5.35. Small signal output conductance and unity gain cut-off frequencies versus drain voltage for the 0.15μm gatelength, double-doped JHEMT with source-to-drain spacing of 2μm. The current gain cut-off frequency was measured using a network analyzer, and the power gain cut-off frequency was calculated using equation [5.11].

gate resistance is due to a combination of lower doping in the gate layer ($1x10^{20}$ to $3x10^{19} cm^{-3}$), and the shorter gatelength (0.2 to 0.15μm). The consequence of higher gate resistance is manifested by the severe reduction of f_{max}. Recall, for the single-doped JHEMT (L_g=0.2μm: N_A=$1x10^{20} cm^{-3}$) the f_{max} approached 200GHz at 1V (V_{ds}), whereas the f_{max} of the double-doped JHEMT (L_g=0.15μm: N_A=$3x10^{19} cm^{-3}$) is 130GHz at 1V (V_{ds}).

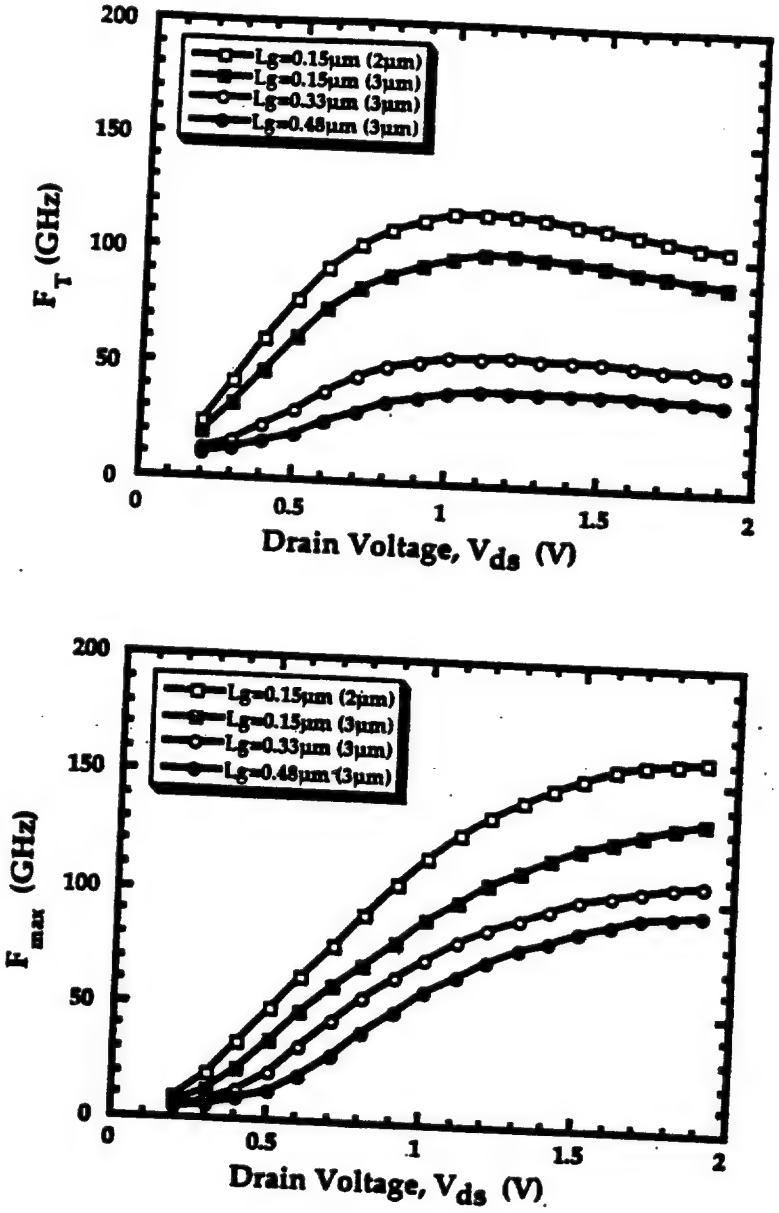


Figure 5.36. f_T and f_{max} versus drain voltage 0.15μm (L_{sd}=2μm), 0.15μm (L_{sd}=3μm), 0.33μm, and 0.48μm gatelength, double-doped JHEMTs. The higher f_{max}/f_T ratio for the longer gatelength devices is indicative of the decreasing gate resistance for the longer gatelengths.

References

[1] Based upon the back depletion of 120Å for a gate doped at $5x10^{18}$ cm^{-3}, and 6Å for a gate layer doped at $1x10^{20}$ cm^{-3}. The remainder of the gate-to-2DEG is calculated using the layer thicknesses from wafer #V1307.

[2] The surface depletion may be determined using Figure D.1 in Appendix D, and the back depletion is calculated from equation [2.31] using the donor sheet density of $6x10^{12}cm^{-2}$.

[3] L.D. Nguyen, A.S. Brown, M.A. Thompson, and L.M. Jelloian, "50-nm Self-Aligned-Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," IEEE Trans on Electron Dev., Vol 39, No. 9, Sept. 1992

[4] This effect is due to the violation of the Lever Rule which states that the barrier layer must be much thicker than the spacer layer in order to maintain a high channel electron concentration. Clearly, as the electron concentration is reduced, and the sheet resistance increases. See Chapter 2, section 2.1.

[5] *Quantum Mechanics*, H. Kroemer, (Prentice Hall, Englewood Cliffs, New Jersey, 1994) Chapter 5.

[6] *Bandprof*, W.R. Frensley, University of Texas at Dallas.

[7] Y. Suzuki, H. Hida, H. Toyoshima, and K. Ohata, "High Speed Ring Oscillators using Planar p^+-Gate n-AlGaAs/GaAs 2DEG FETs," Electron. Lett. Vol. 22, No. 12, pp. 672-673, June 1986.

[8] B. Hughes and P.J. Tasker, "Bias Dependence of the MODFET Intrinsic Model Element Values at Microwave Frequencies," IEEE Trans. on Electron Devices, Vol. 36, No. 10, October 1989.

[9] B. Hughes and P. Tasker, "Scaling of Parasitics in mm-Wave MODFETs," SPIE, Vol. 1288, Pg. 227, 1990.

[10] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, " A New Method of Determining the FET small-signal Equivalent Circuit," IEEE Trans. Microwave Theory Tech., Vol. 36, pp. 1151-1159, July 1988.

[11] The simplified model in Figure 5.17 neglects the depletion capacitance and any resistance from the gate contact to the source resistance.

[12] Recall, G_{max} may be written as $\left(R_n/4\cdot(R_g+R_m+R_s)\right)\cdot\left(f_T/f\right)^2$. Of course, in this statement it is assumed that the extrinsic gate and source resistance are not overwhelmingly large.

[13] Recall, the output terminals of the two-port network are shorted.

[14] Clearly, intrinsic simply means that the parasitic y- and z-parameters are subtracted from the measured s-parameters before converting to h-parameters.

[15] P.J. Tasker and B. Hughes, "Importance of Source and Drain Resistance to the Maximum f_t of millimeter-wave MODFETs," IEEE Electron Dev. Lett., Vol. 10, July 1989.

[16] S. Sze, *Physics of Semiconductor Devices*, John Wiley Publishing, 1981.

[17] R.A. Pucel, H.A. Hauss, and H. Statz, "Signal and Noise Properties of GaAs Microwave FET," Advances in Electronic and Electron Physics, Vol. 38, L. Morton Ed., New York: Academic, 1975.

[18] H. Fukui, "Design of microwave GaAs MESFET's for Broadband, Low-Noise Amplifiers," IEEE Trans. Microwave Theory Tech., Vol. MTT-27, pp. 643-650, July 1979.

[19]M.W. Pospieszalski, "Model of Noise Parameters of MESFET's and MODFET's and their Frequency and Temperature Dependence," IEEE Trans. Microwave Theory Tech., Vol. 37, pp. 1340-1350, Sept. 1989.

[20] It should be noted that this value is well into the suspected noise floor of the system.

[21] K. Ohata, H. Hida, and H. Miyamoto, M. Ogawa, T. Baba, and T. Mizutani, "A low-noise AlGaAs/GaAs FET with p+ gate and selectively doped structure," in IEEE Int. MTT-S Microwave Symp. Dig., pp. 434-436, 1984.

[22] The increase in doping while reducing the donor layer thickness approaches the implementation of planar doping which inherently has lower mobility for thinner spacer layers (see Figure 5.3)

Chapter 6
Conclusion

6.1 Summary

This investigation focused on the gate region of the InP-based HEMT. There are two distinct advantages of the JHEMT over the Schottky HEMT. First, the fixed gate-to-channel separation of the JHEMT determines important device parameters (e.g. V_{th}, C_{gs}, and G_{ds}) which vary with the gate recess in the Schottky HEMT. Second, the gate barrier of the JHEMT may be tailored (by selecting a gate material whose energy bandgap determines the gate barrier) to reduce electron injection from the gate into the channel. By comparison, the gate barrier of the InP-based Schottky HEMT is low (0.6eV) and varies with applied gate bias (due to weak pinning of the surface Fermi Level).

In addition, the selection of the gate material of the JHEMT also determines other relevant parameters (e.g. gate contact resistivity, acceptor doping capability) which affect important aspects of the device. The trade-offs are the underlying focus in the following summary of the JHEMTs reported in this work.

The two gate materials investigated were p^+-GaInAs (E_g=0.75eV) and p^+-AlInAs (E_g=1.48eV). A summary of the advantages and disadvantages of each material is given in Figure 6.1. If p^+-AlInAs is chosen as the gate layer, then a large gate barrier is achieved which is suitable for enhancement-mode operation. But, the high barrier comes at

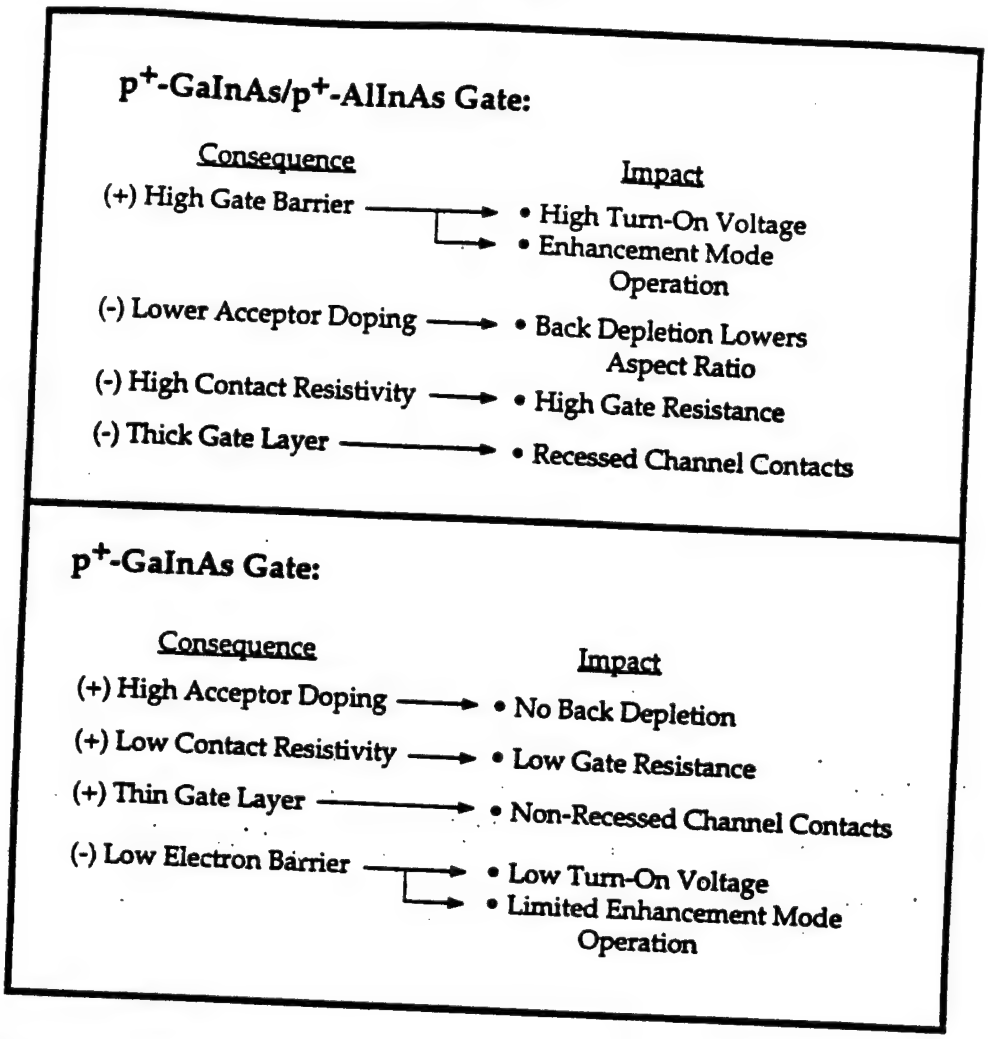


Figure 6.1. Consequences and Impact of choosing either p^+-GaInAs/p^+-AlInAs or p^+-GaInAs as the gate material for the JHEMT.

the expense of (i) high gate contact resistivity ($4x10^{-6}\ \Omega \cdot cm^2$), (ii) gate back depletion (120Å) which effectively reduces the aspect ratio, and (iii) a thick gate region (~600Å) since the AlInAs requires a graded transition to a p^+-GaInAs cap layer. However, if p^+-GaInAs is chosen as the gate layer,

then the barrier is compromised to achieve (i) lower gate contact resistivity ($3x10^{-7}\ \Omega \cdot cm^2$), (ii) negligible gate back depletion (6Å), and (iii) a thin gate region (~200Å) since the p+-GaInAs is also the cap layer.

The gate barrier height of the JHEMT is uniform (solely determined by the MBE growth) resulting in high threshold voltage uniformity ($\sigma(V_{th})$=13.7mV). A one-dimensional charge control model which is consistent with experimental data, was developed to predict the threshold voltage of the JHEMT. The influence of the aspect ratio on the threshold voltage is reflected in the threshold voltage shift of 200mV by varying the gatelength from 0.48 to 0.15μm.

Non-alloyed regrown contacts and alloyed contacts were competing ohmic contact technologies. In 1μm gatelength JHEMTs, the regrown ohmic contact produced a 40% and 75% higher off-state and on-state breakdown voltage, respectively, compared to alloyed ohmic contacts with similar contact resistance. The lowest contact transfer resistance achieved for non-alloyed and standard alloyed ohmic contacts was 0.53 and 0.2Ω-mm, respectively. Alloyed ohmic contacts were preferred for the mm-wave devices in this work because high contact transfer resistance (obtained for non-optimized regrown contacts) translates into excessive parasitic transit delay.

For the 0.2μm gatelength p+-AlInAs JHEMT with regrown ohmic contacts, the high parasitic transit delay and low intrinsic capacitance (0.6pF/mm) limited the unity current gain cut-off frequency (f_τ) to 62GHz. Further, the triangular-shaped gate ($\frac{R_{sq}}{W}$=820Ω/mm) contributed

to the low unity power gain cut-off frequency (f_{max}) of 110GHz. For the 0.2μm gatelength p+-GaInAs JHEMT with alloyed ohmic contacts, the reduced parasitic delay and high intrinsic capacitance (0.85pF/mm) improved the f_τ to 105GHz. The high gate layer doping ($1x10^{20} cm^{-3}$) and T-shaped gate ($\frac{R_{sh}}{W}$=250Ω/mm) translated into a lower extrinsic gate resistance (0.91Ω-mm) and a high f_{max} (greater than 200GHz). State-of-the-art minimum noise figure (F_{min}=0.45dB) and associated gain (G_a=14.5dB) are also achieved. A double-doped, p+-GaInAs JHEMT with 0.15μm gatelength exhibited 20% higher current density (550mA/mm) and 12% higher unity current gain cut-off frequency (118GHz). The lower f_{max} of the double-doped JHEMT is due to the lower acceptor doping employed in the gate layer ($3x10^{19} cm^{-3}$)

Finally, the transport analysis of the p+-GaInAs/n-AlInAs/GaInAs JHEMT diode suggests that the forward bias gate current is dominated by electrons whose energy is less than the peak of the gate potential barrier. This phenomenon is responsible for the lower turn-on voltage (0.57V) observed in these devices and was predicted by our analysis.

6.2 Suggestions for Future Work

(A) Wafer-to-Wafer Threshold Voltage Uniformity

Several authors have reported excellent threshold uniformity across one wafer[1,2,3]. Recall, the threshold voltage of the JHEMT is determined by the growth, whereas the other methods rely on processing reproducibility to achieve threshold voltage uniformity. The

reproducibility of device characteristics (including threshold voltage) from run-to-run will determined the sensitivity of the circuits designed with this technology. Therefore, wafer-to-wafer threshold voltage uniformity is perhaps a more important figure of merit and deserves investigation.

(B) Reverse Gate Leakage

The reverse gate leakage current drifted when the devices were stored for a period of several weeks. Also, kinks in the reverse leakage characteristic were observed where the leakage current would increase linearly (around V_{gs}=-1V), then saturate. A two-dimensional transport model of the gate diode is suggested to fully understand the reverse leakage components and how the surface contributes to the leakage current.

(C) Reliable Access Region Etching

Inherently, the gate region of the JHEMT is fixed at the expense of defining the access regions during the fabrication. As shown in this work, the resistance of the access region can vary significantly depending on the uniformity of the recess etch. The varying sheet resistance can cause deviations in full channel current, transconductance, and source resistance. Therefore, the utilization of an InP stop etch layer or a selective wet chemistry is suggested to improve the access resistance uniformity.

(D) Enhancement-Mode p$^+$-AlInAs JHEMT

For applications (e.g. mobile communications) where only a positive battery supply is available, enhancement mode devices are preferred. As shown in Figure 6.1, p$^+$-AlInAs is the preferred gate

material for enhancement mode operation. A schematic of an enhancement mode p^+-AlInAs JHEMT structure is shown in Figure 6.2. The access regions require n^+ regions which can be readily regrown by MOCVD. These regions must be formed adjacent to the intrinsic region of the device to avoid excessive parasitic resistance. The enhancement mode, p^+-AlInAs gate JHEMT is the III-V version of the enhancement mode Si-MOSFET.

(E) Improved Design for Depletion-Mode p^+-GaInAs JHEMTs

The high aspect ratio design of the p^+-GaInAs JHEMT requires a thin barrier layer . A thin barrier layer reduces the number of electrons

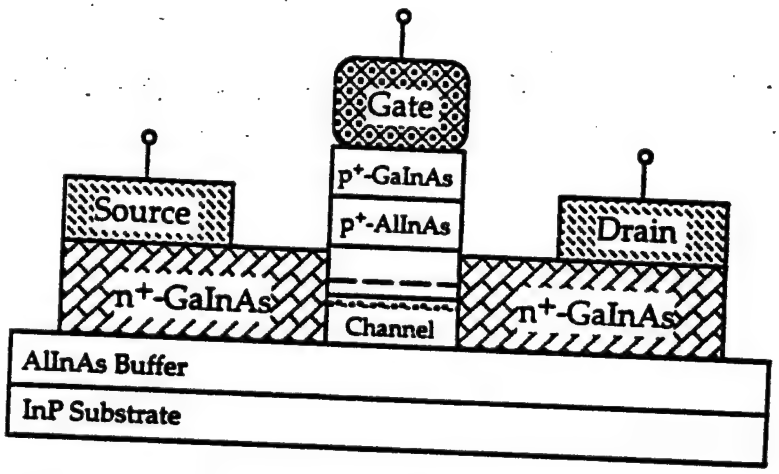


Figure 6.2. Schematic of an enhancement mode, p^+-AlInAs gate JHEMT with regrown access regions. The n^+-material in the access regions is employed to reduce the source and drain resistance and provide high current drive capability.

which transfer from the donor layer to the channel according to the *Lever Rule*. To increase the channel electron concentration in the access regions, the surface potential is absorbed using an n-type regrown surface layer as shown in Figure 6.3. Furthermore, a wide-bandgap material (e.g. GaP) is proposed in order to reduce surface leakage. The higher sheet charge of this proposed structure reduces the input resistance and improves the current drive capability.

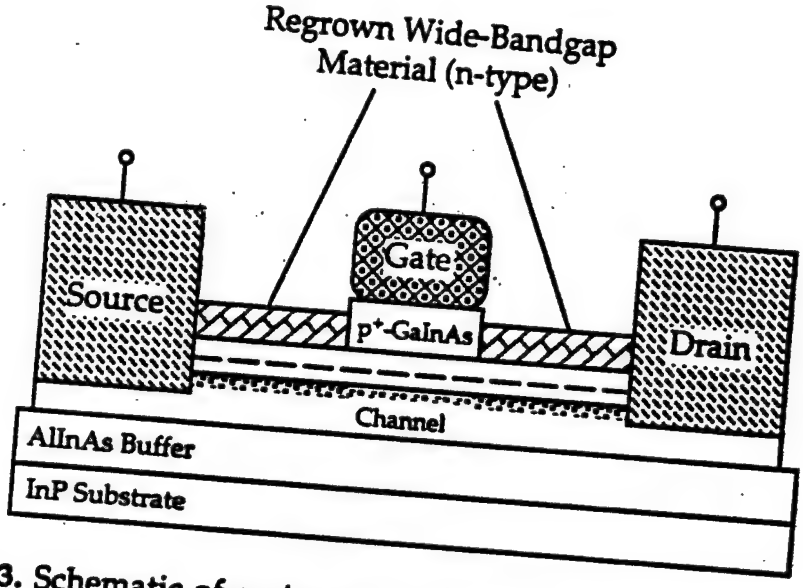


Figure 6.3. Schematic of an improved depletion-mode, P+-GaInAs gate JHEMT with regrown wide-bandgap surface layer. The regrown layer is designed to absorb the surface potential, resulting in lower sheet resistance in the access regions.

References

[1] M. Tong, K. Nummila, A. Ketterson, I. Adesida, C. Caneau, and R. Bhat, "InAlAs/InGaAs/InP MODFET's with Uniform Threshold Voltage Obtained by Selective Wet Gate Recess," IEEE Electron Dev. Lett., Vol. 13, No. 10. Oct. 1992.

[2] T. Aigo, A. Jono, A. Tachikawa, R. Hiratsuka, and A. Moritani, "High uniformity of threshold voltage for GaAs/AlGaAs high electron mobility transistors grown on a Si substrate," Appl. Phys. Lett. Vol. 64, No. 23, June 6 1994.

[3] H. Ishikawa, H. Shibata, and M. Kamada, "Excellent Uniformity of threshold voltage of Si-planar-doped AlInAs/GaInAs heterointerface field-effect transistors grown by metalorganic chemical vapor deposition," Apply. Phys. Lett., Vol. 57, No. 5, July 30 1994.

Appendix A
JHEMT Lumped Element Approximation

The use of a junction to modulate the 2-DEG introduces an extra gate resistance, in addition to the metal gate resistance, corresponding to the contact resistance of the gate-electrode to the p-type gate region. For sub-micron gate length JHEMTs, both resistances significantly contribute to the overall input impedance. The transmission line model proposed by Wolf is modified in order to account for the additional resistance in the JHEMT. The input impedance of the new transmission line is then approximated by a power series expansion and a lumped-element approximation of the JHEMT is obtained.

JHEMT Input Impedance Model

Since the input signal applied from the feeding end of the gate propagates along the gate metallization to the other end, the gate has to be analyzed as a distributed network. The distributed network of the JHEMT is shown in Figure A.1, where we have defined the following infinitesimal quantities:

$$dR_{g1} = \left(\frac{R_m}{W}\right) \cdot \frac{dx}{n^2} \qquad [A.1]$$

$$dR_{g2} = \frac{\rho_c}{L_g \cdot dx} \qquad [A.2]$$

$$dC_{gs} = \left(\frac{C_g}{A}\right) \cdot L_g \cdot dx \qquad [A.3]$$

The factor R_m/W is the gate metal end-to-end resistance per unit length

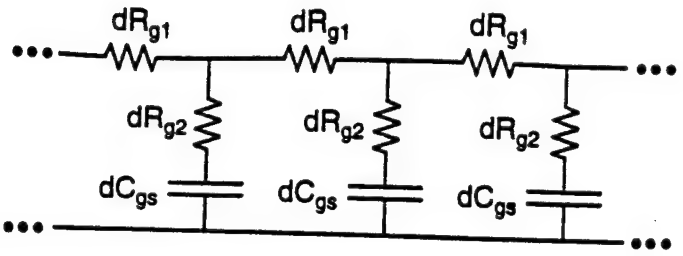


Figure A.1. Distributed input impedance network of a JHEMT.

---

in Ω/mm. The factor $1/n^2$ (where n is the number of gate fingers) arises from utilizing a parallel combination of gate fingers. The term ρ_c is the contact resistivity (Ω-cm^2) of the gate metal to the p-doped gate region. Finally, the factor C_g/A is the gate capacitance per unit area in F/cm^2.

The unit cell is re-expressed in terms of a single series-impedance along with a single shunt-admittance where we have defined:

$$Z = dR_{g1} = \left(\frac{R_m}{W}\right)\cdot\frac{dx}{n^2} \qquad [A.4]$$

$$Y = \frac{1}{dR_{g2} + \dfrac{1}{j\omega\cdot dC_{gs}}} = \frac{j\omega\cdot\left(\dfrac{C_g}{A}\right)\cdot L_g\cdot dx}{1 + j\omega\cdot\rho_c\cdot\left(\dfrac{C_g}{A}\right)} \qquad [A.5]$$

Applying the telegraphers equations for an open-circuit transmission line of length, W, the transmission line network can be essentially modeled as:

$$Y_{in} = Y_o \tanh(\gamma W) \qquad [A.6]$$

where the characteristic admittance of the transmission line, Y_o, may be written as

$$Y_s = \sqrt{\frac{Y}{Z}} = \sqrt{\frac{j\omega \cdot \left(\frac{C_g}{A}\right) \cdot L_g \cdot W}{\left(\frac{R_m}{W}\right) \cdot \frac{W}{n^2} \cdot \left[1 + j\omega \cdot \rho_C \cdot \left(\frac{C_g}{A}\right)\right]}} \qquad [A.7]$$

and the electrical length of the transmission line, γW, is given by

$$\gamma W = \sqrt{Y \cdot Z} \cdot W = \sqrt{\left(\frac{R_m}{W}\right) \cdot \left(\frac{W}{n^2}\right) \cdot \frac{j\omega \cdot \left(\frac{C_g}{A}\right) \cdot L_g \cdot W}{\left[1 + j\omega \cdot \rho_c \cdot \left(\frac{C_g}{A}\right)\right]}} \qquad [A.8]$$

Now, if we define the following total quantities

$$R_{g1} = \left(\frac{R_m}{W}\right) \cdot \frac{W}{n^2} \qquad [A.9]$$

$$R_{g2} = \frac{\rho_c}{L_g \cdot W} \qquad [A.10]$$

$$C_{gs} = \left(\frac{C_g}{A}\right) \cdot L_g \cdot W \qquad [A.11]$$

then we can simplify [A.7] and [A.8] to obtain

$$Y_s = \sqrt{\frac{j\omega C_{gs}}{R_{g1} \cdot \left[1 + j\omega \cdot R_{g2} \cdot C_{gs}\right]}} \qquad [A.12]$$

and

$$\gamma W = \sqrt{\frac{j\omega \cdot R_{g1} \cdot C_{gs}}{\left[1 + j\omega \cdot R_{g2} \cdot C_{gs}\right]}} \qquad [A.13]$$

Next, we assume the phase angle is small and expand [A.6] using the following approximation:

$$\tanh(x) \approx x - \frac{x^3}{3} \quad \text{for } x << 1 \qquad [A.14]$$

thus, we obtain:

$$Y_{in} = Y_o \cdot \gamma W \cdot \left(1 - \frac{(\gamma W)^2}{3}\right) \quad \text{for } |\gamma W| << 1 \qquad [A.15]$$

The assumption that the electrical length of the transmission line must remain small imposes an upper limit on the allowable frequency in [A.13].

Now substituting [A.12] and [A.13] into [A.15], we obtain the following simplified form (after simple mathematical manipulation):

$$Y_{in} = \frac{\left(1 - 2j\omega R_{g2} C_{gs} + \omega^2 R_{g2}^2 C_{gs}^2\right)\left[\omega^2 C_{gs}^2\left(\frac{R_{g1}}{3} - R_{g2}\right) + j\omega C_{gs}\right]}{\left(1 + \omega^2 R_{g2}^2 C_{gs}^2\right)^2} \qquad [A.16]$$

After expanding the numerator we separate real and imaginary terms to determine the equivalent conductance and susceptance. More simply stated, we write [A.16] in the following form:

$$Y_{in} = G + jB \qquad [A.17]$$

where

$$G = \frac{\omega^2 C_{gs}^2\left[2R_{g2} + \left(\frac{R_{g1}}{3} - R_{g2}\right)\left(1 + \omega^2 R_{g2}^2 C_{gs}^2\right)\right]}{\left(1 + \omega^2 R_{g2}^2 C_{gs}^2\right)^2} \qquad [A.18]$$

and

$$B = \frac{\omega C_{gs}\left[1 + 2\omega^2 R_{g2}^2 C_{gs}^2 - \omega^2 \frac{R_{g1}}{3} R_{g2} C_{gs}^2\right]}{\left(1 + \omega^2 R_{g2}^2 C_{gs}^2\right)^2} \qquad [A.19]$$

Now, it is assumed that $\omega^2 R_{g2}^2 C_{gs}^2 << 1$, which states that the RC time constant of the gate contact resistance and the gate capacitance must be small compared to $1/\omega$. Applying this constraint we obtain the following admittance and susceptance:

$$G = \omega^2 C_{gs}^{\,2}\left[\frac{R_{g1}}{3} + R_{g2}\right] \qquad [A.20]$$

$$B = \omega C_{gs} \qquad [A.21]$$

$$\text{for } \omega << \frac{1}{R_{g1} \cdot C_{gs}} \text{ and } \omega << \frac{1}{R_{g2} \cdot C_{gs}}$$

For inclusion into a small-signal circuit model, the impedance network is a more convenient form. The equivalent impedance network is readily calculated from [A.20] and [A.21]:

$$Z_{in} = R + jX \qquad [A.22]$$

where the lumped element resistance and susceptance are

$$R = \frac{R_{g1}}{3} + R_{g2} \qquad [A.23]$$

$$X = \frac{1}{\omega C_{gs}} \qquad [A.24]$$

$$\text{for } \omega << \frac{1}{R_{g1} \cdot C_{gs}} \text{ and } \omega << \frac{1}{R_{g2} \cdot C_{gs}}$$

The lumped element equivalent, input impedance network is given in Figure A.2.

Consistent with Wolf's analysis, we obtain the same reduced value of metallization resistance (one-third of the end-to-end dc resistance) and the gate-to source capacitance. Further, an additional resistance associated with the ohmic contact to the p-type region, R_{g2} is also obtained. The magnitude of this resistance is proportional to the specific contact resistance of the gate and inversely proportional to the gate length as shown in from [A.10].

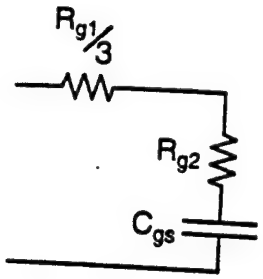


Figure A.2. Lumped-element equivalent gate input impedance network of the JHEMT.

Appendix B
MOCVD Doping Behavior

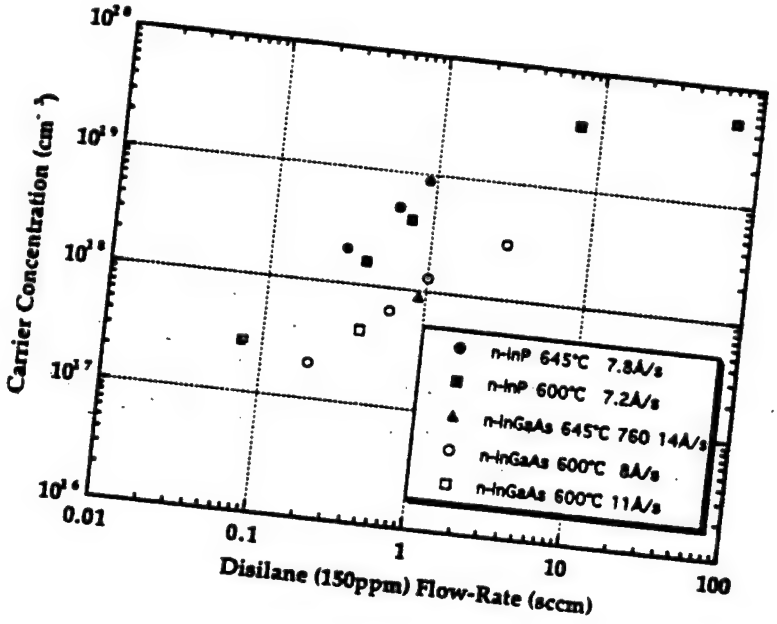
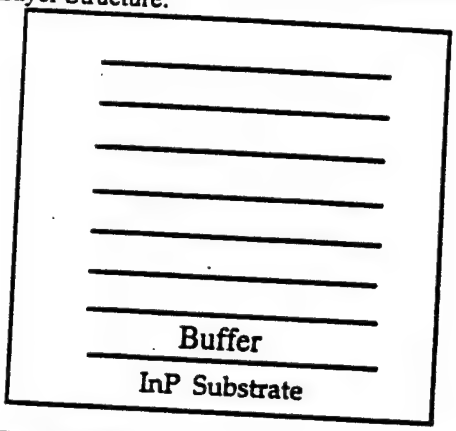


Figure B.1. Doping Concentration versus Flow Rate of the disilane/hydrogen mixture. The carrier concentrations were meaure at room temperature. (courtesy S. Denbaars)

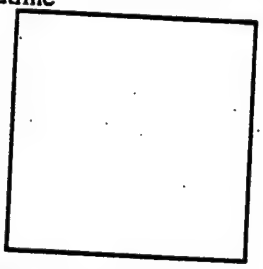
Appendix C
JHEMT Process Traveler

WAFER # _____

Layer Structure:



Sample outline



MASK USED: **vers. 8-1-94**

O..... PWR JHEMT Mask Set
O..... MEMS3 Mask Set
O..... Other: _____

Microscope: color, morphology, etc

OHMIC

1. Clean: ACE, IPA, N2 Dry
2. Dehydration bake @180° 30 sec. on HP
3. Spin PR Shipley 1400-27D1
4. Softbake
   O Hotplate @70°C 30sec
5. Expose Pattern:

O.....t= XXsec @ 20mW/cm2
O.....t= _____
6. Image Reversal: Recipe #2 (1.75Hrs.)
7. Flood: Xmin @20mW/cm2
8. Develop: MF312:DI (3:4)
O.....t= XX sec
O.....t=_____
9. Inspect: double check edge quality
10. Descum: O2 plasma LF-5
Run # _____
11. Oxide etch: BOE (7:1)
O t= Xsec
O t=_____
12. Evaporate: O Ni/ AuGe/Au
O _____
thickness:
O X00Å/X00Å/X000Å
O.....

Run# _____
Temescal# _____

13. Liftoff in Acetone, IPA, DI , N2 Dry
14. Inspect

IMPLANT ISOLATION

1. Clean: ACE, IPA, N2 Dry
2. Dehydration bake @180° 30 sec. on HP
3. Spin PR Shipley 1375
4. Softbake
O Oven @70°C 30min
O Hotplate @70°C 30sec
5. Expose Pattern:
O.....t= XXsec @ 20mW/cm2
O.....t= _____
6. Image Reversal: Recipe #2 (1.75Hrs.)
7. Flood: Xmin @20mW/cm2
8. Develop: MF312:DI (3:4)
O.....t= XX sec
O.....t=_____
9. Inspect: double check edge quality

IMPLANT

Done By _____
Vacc/Dose/Time

Current _____

time/thickness:

1._____ 5._____
2._____ 6._____
3._____ 7._____
4._____ 8._____

Microscope Comments

_____

ALLOY (TEMP=355°C, t=50sec.)

TEMPERATURE: _____
TIME: _____

SURFACE MORPHOLOGY:

_____

"T" GATE

E-Beam Spinner Parameters:
Use Left Spinner

1. Calibrate Nanospec Using Own Wafer
2. Clean: ACE, IPA, N2 Dry
3. Bake @XXX° for XXmin (L)
4. Spin 1st Bi-Layer:
5. Bake @XXX° for XXmin (R)
6. Nanospec: XXXXÅ +/- XXXÅ

thickness: _____

7. Spin 2nd Bi-Layer:
8. Bake @180° for 30min (R)
9. Nanospec: XXXXÅ +/- XXXÅ

thickness: _____

10. E-Beam Exposure:

Target Gate Length:
- O Lg=0.20μm, T-shape
- O Lg=_____

Gate-Source Spacing:
- O Lgs=0.5μm
- O Lgs=_____

Exposure Log# _____

Pattern Name _____

Comments:

11. Inspection:

Approximate Dimensions:

L_g= _____

L_T= _____

Comments:

12. Descum: O_2 plasma LF-5
Run # _____
13. Oxide etch: BOE (7:1)
O t= Xsec
O t= _____
14. Evaporate: O Ti/Pt/AuNi
O _____
thickness:
O X00Å/X00Å/X000Å/X000Å
O..... _____

Run# _____
Temescal# _____

14. Liftoff in Meth-Clrorine 38-40°, XXmin
15. Rinse in ACE, IPA, N2 Dry
15. Inspect

MESA ISOLATION

Wet

1. Clean: Ace, Iso
2. Dehydration bake @120° 10min
3. Spin PR P4110 6K 30sec
4. Softbake Oven @90°C 10min
5. Expose Edges 1min
6. Develop Edges 1:4 AZ400K:DI 20+20sec
7 Align / Expose; Intensity= _____ mW/cm^2
O.....t= 8sec
[O.....t= _____]
8. Develop AZ400K:DI 1:4
O.....t= 40 sec
[O.....t= _____]
9. Verify development under microscope
10. Descum: O_2 plasma 15sec
11. Hardbake @120°C 15min Oven
12. Etch Mesa:
O Etch With
H_3PO_4: H_2O_2:DI ; 3:1:50

time/thickness:

1._____ 5._____
2._____ 6._____
3._____ 7._____
4._____ 8._____

Microscope Comments:

Gate Recess (Access Region) Etch:

1. Descum: O_2 plasma LF-5
   100W-0.2T-2min: Run # _____
2. Oxide etch: 1:15, NH4OH:DI
   - O t= 10sec
   - O t=_____
3. Etch Access Region:
   - O Etch With
     H_3PO_4:Citric:H_2O_2:H_20
     (1:100:10:400)

time/thickness:

1._____ 5._____
2._____ 6._____
3._____ 7._____
4._____ 8._____

OVERLAY

1. Clean: ACE, IPA, N2 Dry
2. Dehydration bake @180° 30 sec. on HP
3. Spin PR Shipley 1400-27D1
4. Softbake
   - O Oven @70°C 30min
   - O Hotplate @70°C 30sec
5. Expose Pattern:
   - O.....t= 16sec @ 20mW/cm2
   - O.....t= _____
6. Image Reversal: Recipe #2 (1.75Hrs.)
7. Flood: 6min @20mW/cm2
8. Develop: MF312:DI (3:4)
   - O.....t= XX sec
   - O.....t=_____
9. Inspect: double check edge quality
10. Descum: O_2 plasma LF-5
    Run # _____
11. Oxide etch: BOE 7:1
    - O t= Xsec
    - O t=_____

12. Evaporate: O Ti /Pt/Au
    O _____
    thickness:
    O 1000Å/1000Å/3000Å
    O....._____

    Run# _____
    Temescal# _____

13. Liftoff in Acetone, IPA, DI , N2 Dry
14. Inspect

TEST WAFER

Appendix D
Surface Depletion

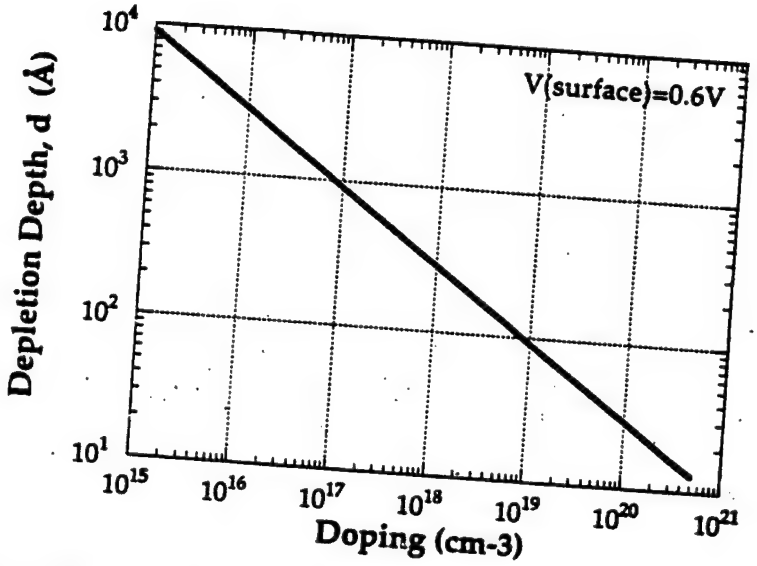


Figure D.1. The depletion extension into a semiconductor region due to an applied surface potential of 0.6V. The independent axis is the doping of the layer adjacent to the surface. The depletion approximation is used in this calculation.

Appendix E
Program Code For Current Calculation

The following code was used to determine the transmission probability and gate current:

```
10! Scattering Matrix Calculations, version 1.0
20! Function: This program calculates the I-V characteristics of
30!         modulation-doped heterostructures.
40!         # This software currently supports AlInAs and GaInAs
50!          heterostructures.
60! Written by Jeff Shealy
70! Last modication, Saturday 10-29-94
80!
90  GINIT
100  GCLEAR
110  GRAPHICS ON
120  OPTION BASE 1
130  OUTPUT 2;"K"
140  ALLOCATE W$(1:30)[10],Title$[80],St$[1]
150  MAT W$= (RPT$(" ",10))
160  CLEAR SCREEN
170!
180  CONTROL 1,12;0
190  CONTROL 2,2;1
200  CONTROL 2,14;0
210!
220  COM /Info/ Date$[11],Time$[8],Xlabel$[6],Ylabel$[12]
230  COM /Const1/ REAL Qe,Eps0,Kb,Ao,Eps1,Eps2
240  COM /Const2/ INTEGER Temp
250  COM /Const3/ REAL Plank,Hbar
260  COM /Const4/ REAL Mo,M1,M2,Mdef
270  COM /Const5/ REAL Tn,Tp
280  !
290  COM /Cntrs/ INTEGER Cb_num,Ld_flag,Clc_flag,Trig
300  !
310  COM /Barr1/ INTEGER Numb,Selected,Scan_start,Scan_stop
320  COM /Barr2/ REAL Linc,Const1
330  COM /Bands/ REAL Ec(1000),Ef(1000),Ev(1000),X(1000),Mstar(1000)
340  COM /Band2/ REAL Lx(1000),V(1000),E_field(1000)
350  COM /Band3/ REAL Edonor_min,Edonor_index
360  COM /Band3/ INTEGER Out_flag,Varz
370  !
380  COM /Prop1/ COMPLEX Pt(2,2),Pd(2,2),Pf(2,2),P(2,2)
390  COM /Prop2/ COMPLEX Pu,Pk,Ph,Pkold,Pk_temp
400  COM /Prop3/ REAL De,Ezo,Ez,Beta,Vmax,Ef_ref,Phi_b
```

```
410 !
420 COM /Curr1/ REAL Tot,Class,Vapp
430 COM /Curr2/ REAL Jtot,Jclass,Jtet,Jtfe,Jtet_well,Jtet_p
440 COM /Curr3/ REAL Itot,Ite,Itet,Itfe,Itet_well,Itet_p
450 COM /Curr4/ REAL Tfe_const
460 COM /Curr5/ REAL Trans(200),Jc(200),Jt(200),Ezz(200)
470 COM /Curr6/ REAL Eb_well,Eb_tfe,Eb_ecp
480 !
490 COM /File1/ Infile$[7]
500 COM /Titles/ Codeword$[10]
510 !
520 COM /Auto/ INTEGER T_cntr,V_cntr,Num_cntr
530 COM /Auto2/ Tm$[2],Vm$[3],Formata$[115]
540 COM /Auto3/ REAL J1(6,100),J2(6,100)   ! 6 Temps and 100 Vg's
550 !
560 ! ********************************************************************
570 ! Initialize Vars
580 ! ********************************************************************
590 !
600 Qe=1.6E-19        ! C
610 Eps0=8.85E-14     ! F/cm
620 Temp=300          ! K
630 Kb=1.38E-23       ! J/K
640 Eps1=13.7         ! for GaInAs
650 Eps2=12.7         ! for AlInAs
660 Mo=9.1E-31        ! Kg (free electron mass)
670 M1=.041           ! electron m* ratio for GaInAs
680 M2=.084           ! electron m* ratio for AlInAs
690 Mdef=.1           ! default effective mass ratio
700 Ao=120            ! Richardson's Coef: A*cm-2*K-2
710 Plank=6.62618E-34 ! J*s
720 Hbar=1.05E-34     ! J*s
730 !
740 !
750 Linc=1.0E-9       ! (m), length of each barrier. (10 Angstroms)
760 Ld_flag=0         ! Set load and calc flag to false.
770 Clc_flag=0
780 De=.01            ! (ev) incremental energy
790 Scan_stop=150     ! number of energies to scan
800 Scan_start=1
810 Codeword$=" CHANNEL"
820 !
830 MAT Ef= (0)
840 MAT X= (0)
850 MAT Ec= (0)
860 MAT Ev= (0)
870 MAT V= (0)
```

```
 880  MAT J1= (0)
 890  MAT J2= (0)
 900  !
 910  ! ************************************************************
 920  ! Start Program
 930  ! ************************************************************
 940 Menu: !
 950  CLEAR SCREEN
 960 Menu2:  !
 970  Choice=0
 980  W$(1)=" LoadBand "
 990  W$(2)=" Current "
1000  W$(3)=" SaveData "
1010  W$(4)=" **EXIT** "
1020  W$(5)="  Auto  "
1030  W$(6)=""
1040  W$(7)=""
1050  W$(8)=""
1060  W$(9)=""
1070!
1080  Title$="Scatt Main Menu"
1090  Choice=FNChoice(W$(*),Title$,Choice)
1100  SELECT Choice
1110  !_____________________________________________________
1120  CASE 1        !This case loads DOS file containing the bands.
1130  !
1140  ! 1) Ask user to tell how many points to expect (cb_num)
1150  ! 2) Set Ezo equal to the Ecmin (from the input file).
1160  ! 3) Set Vmax equal to the Ecmax (from the input file).
1170  ! 4) Ask the user to furnish an applied bias, i.e. Vapp=?
1180  ! 5) Set effective mask in array M*.  Use Eg difference in
1190  !    material to assign values for AlInAs and GaInAs.
1200  ! 6) Plot the conduction band to simulate.
1210  ! 7) From the index of Ezo begin calculations.
1220  !          Note: x(selected)<cb_num
1230  !                x(selected_init)=Ecmin=Ezo
1240  ! 8) Set L=0 at x(selected) and at x=0
1250  !
1260  ! Limits of input file: 1000pts
1270  !                e.g. total layer thickness=1um if discete
1280  !                     layer length is 10 Angstroms.
1290  !
1300  ! Note: To read input file:
1310  !          1) Using vi editor change all spaces to commas or else
1320  !             numbers will be read incorrectly.
1330  !          2) FTP using PC and NOT the Mac or else line terminators
1340  !             are lost.
```

```
1350 !       3) Copy file to current basic directory making sure the
1360 !            name is no longer than 7 letters.
1370 !
1380 !--- --- --- --- --- --- --- ---
1390 !
1400 !
1410  CLEAR SCREEN
1420  INPUT "Enter the name of the band file to read?",Infile$
1430  INPUT "Enter the TEMPERATURE ?",Temp$
1440  IF Temp$<>"" THEN
1450   Temp=VAL(Temp$)
1460  END IF
1470  PRINT USING "K,K";"The file to be read is: ",Infile$
1480  PRINT USING "K,SDDD";"Temperature:",Temp
1490  PRINT USING "K";"-------------------------"
1500  ASSIGN @File TO Infile$&":DOS,D"
1510  !
1520  INPUT "How thick is the layer structure to entered (in nm)?",Cb_num
1530  Cb_num=Cb_num+1          ! accounts for x=0 point.
1540  !
1550  DISP "Reading from file..."
1560  FOR W=1 TO Cb_num
1570   ENTER @File USING "K";X(W),Ev(W),Ec(W)  !Works w/ comma delimin.
1580   !PRINT X(W),Ev(W),Ec(W)
1590  NEXT W
1600  !
1610  ! ***************************************************************
1620  ! Define an electric field as -(E2-E1)/(x2-x1).
1630  E_field(1)=0
1640  FOR Q=2 TO Cb_num
1650   E_field(Q)=(-1)*(Ec(Q)-Ec(Q-1))/(Linc*100)     !V/cm
1660  NEXT Q
1670  !
1680  ! ***************************************************************
1690  ! Find the min/max values of Ec, also make the index of the min
1700  ! value equal to "selected".
1710  DISP "Scanning data..."
1720  Ezo=MIN(Ec(*))
1730  Vmax=MAX(Ec(*))
1740  PRINT "Ecmax=",Vmax
1750  PRINT "Ecmin=",Ezo
1760  !
1770  ! ***************************************************************
1780  ! Find the the index of the Emin.
1790  T=1
1800  Trig=0
1810  REPEAT
```

```
1820   !PRINT T
1830   IF Ec(T)=Ezo THEN
1840    Selected=T
1850    !PRINT "Selected= ",Selected
1860    Trig=1
1870   END IF
1880   T=T+1
1890  UNTIL Trig
1900  !
1910  IF Selected>Cb_num THEN     ! Make sure selected<cb_num
1920   BEEP
1930   DISP "ERROR:Selected index > than index existing from the input file!"
1940   INPUT J$
1950   GOTO Menu
1960  END IF
1970  Numb=Selected      !Numb is the index of Ecmin.
1980  ! ***************************************************************
1990  ! Find the index where Ec is minimum in the donor layer.
2000  Varz=Numb              ! Start counting from (Numb-1) index
2010  Out_flag=0
2020  REPEAT
2030   PRINT "varz=",Varz
2040   Varz=Varz-1
2050   IF Ec(Varz-1)>Ec(Varz) THEN    ! If Ec goes up then found min.
2060    Out_flag=1
2070    Edonor_min=Ec(Varz)
2080    PRINT "Edonor_min=",Edonor_min
2090    Edonor_index=Varz
2100    PRINT "Edonor_index=",Edonor_index
2110   END IF
2120  UNTIL Out_flag
2130  ! ***************************************************************
2140  ! Ask user to input the applied voltage.
2150  BEEP
2160  INPUT "Enter the Applied Gate Voltage (V)?:",Vapp
2170  !PRINT
2180  !PRINT USING "K,K";"The applied gate bias is: ",Vapp
2190  !PRINT
2200  !
2210  ! ***************************************************************
2220  ! Ask the user whether he/she wishes to start counting from
2230  ! channel or from donor region.
2240  Junk$="Z"
2250  INPUT "Calculate from donor level (D) or channel [default]?",Junk$
2260  IF Junk$="D" OR Junk$="d" THEN
2270   Ezo=Edonor_min
2280   Numb=Edonor_index
```

```
2290    Codeword$="  DONOR"
2300   END IF
2310   ! ************************************************************
2320   ! Assigning effective mass relations:
2330   DISP "Assigning effective mass values..."
2340   FOR L=1 TO Cb_num       ! Set values of Effective Mass.
2350    Eg_test=Ec(L)-Ev(L)
2360   !PRINT Cb_num,Numb,Eg_test
2370    IF Eg_test<1.1 THEN   ! If Eg<1.1 then the material is GaInAs.
2380     Mstar(L)=M1
2390    ELSE                  ! Else the material is AlInAs.
2400     Mstar(L)=M2
2410    END IF
2420    Lx(L)=Linc            ! Incremental barrier thickness.
2430   NEXT L
2440   !
2450   Lx(1)=0               ! Make the thickness of the in/out
2460   Lx(Numb)=0              ! barriers=zero.
2470   !
2480   ! ************************************************************
2490   ! Create an array for the barriers where the incoming wave
2500   ! is referenced at an arbitrary energy chosen equal to zero.
2510   FOR Q=1 TO Numb
2520    V(Q)=Ec(Q)-Ezo        ! Assign values.
2530   NEXT Q
2540   V(1)=Ev(1)-Ezo         ! Assign surface value of Ec=Efm.
2550   !Edonor_min=Edonor_min-Ezo      !Assign new value of Edon_min.
2560   Phi_b=Vmax             ! Phi_b is (Vmax-Ef).
2570   Vmax=Vmax-Ezo            ! Assign new value of Vmax.
2580   Ef_ref=0-Ezo           ! Assign new value to Ef.
2590   Ezo=0        ! Change reference to zero since all values
2600              ! are with respect to this value and we want
2610              ! the incoming waves have real values of K.
2620   !
2630   DISP "Final Assigned Parameters..."
2640   PRINT
2650   PRINT "X        Ev        Ec      M*     Li      V      E"
2660   FOR L=1 TO Cb_num
2670    PRINT X(L),Ev(L),Ec(L),Mstar(L),Lx(L),V(L),E_field(L)
2680   NEXT L
2690   !
2700   CLEAR SCREEN
2710   CALL Plot(Cb_num,"x(nm)","Energy(ev)",X(*),Ec(*),Ev(*),Ef(*),Tn,Tp)
2720   INPUT "Press enter to continue...",Junk$
2730   !
2740   Ld_flag=1
2750 !_____________________________________________________________
```

```
2760 CASE 2          !This case calcs scatt/matrix and current.
2770 !
2780  CLEAR SCREEN
2790 Plot_calc:  !
2800  CALL Plot(Numb,"x(nm)","Energy(eV)",X(*),V(*),V(*),Ef(*),Tn,Tp)
2810  INPUT "Press enter continue...",Junk$
2820  !
2830  PRINT USING "K,SD.DDD,K,SD.DDD";"Vmax=",Vmax," Ef=",Ef_ref
2840  IF Ld_flag=0 THEN GOTO Menu
2850 !
2860  Beta=(2*Mo*Qe)/(Hbar)^2     !Effective Mass ratio is not included.
2870  Tot=0                  !Initialize total and classical
2880  Class=0                !currents to zero.
2890  Ecc=Ec(Numb)                !Ec at chosen starting point.
2900 !
2910  FOR Z=Scan_start TO Scan_stop
2920   Ez=Ezo+(Z*De)          !Increment the "scan" energy.
2930   Ezz(Z)=Ez
2940  !
2950  !                Ezo should be set to Ecmin
2960  !
2970   Pk_temp=(Mstar(Numb)*Beta*Ez)
2980   Pkold=SQRT(Pk_temp)          !Pkold is the last K, M* is for
2990  !                initial material at X(numb)
3000  !
3010   Pt(1,1)=CMPLX(1,0)          !Initialize the "seed" matrix.
3020   Pt(1,2)=CMPLX(0,0)
3030   Pt(2,1)=CMPLX(0,0)          !Set Equal To Identity Matrix.
3040   Pt(2,2)=CMPLX(1,0)
3050  !
3060  !Order is changed in order to count BACKWARDS from the initial x!
3070   FOR Y=1 TO Numb          ! Num is the number of barriers.
3080   !
3090   J=Numb-(Y-1)          ! Used in order to count backwards.
3100  !
3110   Pu=Mstar(J)*Beta*(Ez-V(J))  ! Vj is the height of jth barrier.
3120  !                Mj is the Mr* of the jth material.
3130   Pk=SQRT(Pu)          ! Pk is the wave number of barrier.
3140   Ph=2*SQRT(Pkold*Pk)          ! Ph is the 1/(coef) of p-matrix.
3150  !
3160   Pd(1,1)=(Pkold+Pk)/Ph     ! Propagation matrix of barrier.
3170   Pd(1,2)=(Pkold-Pk)/Ph
3180   Pd(2,1)=Pd(1,2)
3190   Pd(2,2)=Pd(1,1)
3200  !
3210   P(1,1)=Pt(1,1)*Pd(1,1)+Pt(1,2)*Pd(2,1)   !Calc P(last)*P(barr)
3220   P(1,2)=Pt(1,1)*Pd(1,2)+Pt(1,2)*Pd(2,2)
```

```
3230    P(2,1)=Pt(2,1)*Pd(1,1)+Pt(2,2)*Pd(2,1)
3240    P(2,2)=Pt(2,1)*Pd(1,2)+Pt(2,2)*Pd(2,2)
3250   !
3260    Pf(1,1)=CMPLX(COS(Pk*Lx(J)),-SIN(Pk*Lx(J)))  !Free Space Propag.
3270    Pf(1,2)=CMPLX(0,0)
3280    Pf(2,1)=CMPLX(0,0)
3290    Pf(2,2)=CMPLX(COS(Pk*Lx(J)),SIN(Pk*Lx(J)))
3300   !
3310    Pt(1,1)=P(1,1)*Pf(1,1)+P(1,2)*Pf(2,1)   !Calc P(barr)*P(free)
3320    Pt(1,2)=P(1,1)*Pf(1,2)+P(1,2)*Pf(2,2)
3330    Pt(2,1)=P(2,1)*Pf(1,1)+P(2,2)*Pf(2,1)
3340    Pt(2,2)=P(2,1)*Pf(1,2)+P(2,2)*Pf(2,2)
3350   !
3360    Pkold=Pk          !Make the "present" K the "initial" K
3370   !                  for the next barrier.
3380   NEXT Y             !Go to the next barrier.
3390   !
3400   Trans(Z)=1/((ABS(Pt(1,1)))^2)   !This is the mag of the T-coef.
3410  !PRINT "Trans=",Trans(Z)
3420   !
3430   Vz=SQRT(2*Qe*Ez/(M2*Mo))        !zth component of velocity
3440   !
3450   Const1=((4*PI*(M2*Mo)*Kb*Temp)/Plank^3)*(Trans(Z)/Vz)  !A constant.
3460  !PRINT "const1=",Const1
3470   !
3480  !PRINT "Ez=",Ez," Ef_ref=",Ef_ref
3490   IF Ez<Ef_ref THEN                    !If E(scan) < Ef, then
3500    Stat=Const1*(1+(Qe*(Ef_ref-Ez))/(Kb*Temp))
3510   ELSE                                 !Else, use
3520    Stat=Const1*EXP(Qe*(Ef_ref-Ez)/(Kb*Temp))
3530   END IF
3540  !PRINT "Stat=",Stat
3550   !
3560   IF (Ez+Vapp-Ef_ref)>0 THEN   !Repetitive calculation for I(Trans)
3570    Tot=Tot+(Qe*Vz*Stat*(Qe*De))
3580   ELSE                 !Else, no states are available and Tc
3590    Tot=Tot             !stays the same.
3600   END IF
3610   Jt(Z)=Tot*1.E-4
3620   !
3630   IF Ez>Vmax THEN
3640    Class=Class+(Qe*Vz*Stat*(Qe*De))      !A/m^2
3650   ELSE
3660    Class=Class
3670   END IF
3680   Jc(Z)=Class*1.E-4
3690   !
```

```
3700    DISP "E(scan)=",Ez," Jtot(A/cm2)=",Jt(Z)," Jte(A/cm2)=",Jc(Z)
3710    !
3720  NEXT Z                !Go to the next incremental energy.
3730 !
3740 !Now calculate the currents.
3750 !
3760 Do_calc: !
3770   BEEP
3780   CLEAR SCREEN
3790   PRINT
3800   PRINT
3810   PRINT
3820   PRINT
3830   PRINT
3840   PRINT
3850   PRINT "*****************************************************"
3860   PRINT "T= ",Temp," K  Vapplied=",Vapp,Codeword$
3870 !Total Transmitted current:
3880   Jtot=Tot*1.E-4        ! A/cm2
3890   PRINT "*****************************************************"
3900   PRINT USING "K,SD.3DE,K";"Jtotal=    ",Jtot," A/cm2  [Transmission]"
3910 !
3920 !Classical Current over the barrier:
3930   Jclass=Class*1.E-4    ! A/cm2
3940   PRINT
3950   PRINT USING "K,SD.3DE,K";"Jte(class)= ",Jclass," A/cm2  [Transmission]"
3960 !
3970 !Thermionic Emission Theory: over peak/out of well/over Ec_p...
3980   Jtet=Ao*M2*T^2*EXP(-(Qe*Phi_b)/(Kb*Temp))  !A/cm2
3990   PRINT
4000   PRINT USING "K,SD.3DE,K";"Jtet(peak)= ",Jtet," A/cm2  [Calculated]"
4010   PRINT USING "K,SD.DDD";"      Effective Barrier=";Phi_b
4020   Jtet_well=Ao*M2*T^2*EXP(-(Qe*(V(Numb-1)-Ef_ref))/(Kb*Temp))  !A/cm2
4030   PRINT
4040   PRINT USING "K,SD.3DE,K";"Jtet(well)= ",Jtet_well," A/cm2  [Calc]"
4050   Eb_well=V(Numb-1)-Ef_ref
4060   PRINT USING "K,SD.DDD";"      Effective Barrier=";Eb_well
4070   PRINT USING "K";" J(well) is not applicable for DONOR calculations"
4080   Jtet_p=Ao*M2*T^2*EXP(-(Qe*(V(5)-Ef_ref))/(Kb*Temp))  !A/cm2
4090   PRINT
4100   PRINT USING "K,SD.3DE,K";"Jtet(Ec_p)= ",Jtet_p," A/cm2  [Calculated]"
4110   Eb_ecp=V(5)-Ef_ref
4120   PRINT USING "K,SD.DDD";"      Effective Barrier=";Eb_ecp
4130 !
4140 !Thermionic Field Emission:
4150   Tfe_const=SQRT((Qe*E_field(25))/(4*PI*Eps2*Eps0))
4160   Jtfe=Jtet*EXP((Qe*Tfe_const)/(Kb*Temp))    !must be > Jtet
```

```
4170  PRINT
4180  PRINT USING "K,SD.3DE,K";"Jtfe(peak)= ",Jtfe," A/cm2  [Calculated]"
4190  Eb_tfe=Phi_b-Tfe_const
4200  PRINT USING "K,SD.DDD";"     Effective Barrier=";Eb_tfe
4210  !
4220  !
4230  PRINT "*****************************************************"
4240  PRINT "For a 0.2x50um2 Device..."
4250  PRINT "*****************************************************"
4260  Itot=Jtot*(2.E-5*5.0E-3)   !Amps
4270  PRINT USING "K,SD.3DE,K";"Itotal=    ",Itot," A [Trans]"
4280  Ite=Jclass*(2.E-5*5.00E-3)   !Amps
4290  PRINT USING "K,SD.3DE,K";"Ite(class)= ",Ite," A [Trans]"
4300  Itet=Jtet*(2.E-5*5.00E-3)   !AmpS
4310  PRINT USING "K,SD.3DE,K";"Itet(peak)= ",Itet," A"
4320  Itet_well=Jtet_well*(2.E-5*5.00E-3)   !AmpS
4330  PRINT USING "K,SD.3DE,K";"Itet(well)= ",Itet_well," A"
4340  Itet_p=Jtet_p*(2.E-5*5.00E-3)   !AmpS
4350  PRINT USING "K,SD.3DE,K";"Itet(Ec_p)= ",Itet_p," A"
4360  Itfe=Jtfe*(2.E-5*5.00E-3)   !Amps
4370  PRINT USING "K,SD.3DE,K";"Itfe(peak)  ",Itfe," A"
4380 !
4390  PRINTER IS CRT
4400  Junk$="N"
4410  INPUT "Do you wish to obtain a/another hardcopy?",Junk$
4420  IF Junk$="Y" OR Junk$="y" THEN
4430   PRINTER IS 701
4440   GOTO Do_calc
4450  END IF
4460  !
4470  ! ***************************************************
4480  Clc_flag=1    ! Indicate a calculation has been completed.
4490  CLEAR SCREEN
4500  GOTO Menu2
```

Appendix F
More Bias Dependent Model Parameters

The bias dependent model parameters of the three double-doped JHEMTs (Lg=0.15, 0.33, and 0.48μm,) whose dc characteristics are shown in Chapter 5, are presented. The gate voltage chosen for each device was determined by the gate voltage where the peak transconductance occurs. The fixed gate voltages for the 0.15μm, 0.33μm, and 0.48μm gate, JHEMTs were -0.7V, -0.55V, and -0.45V. The four intrinsic model parameters compared are the transconductance (g_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and the output conductance (G_{ds}). The transconductance and output conductance are shown in Figure F.1. The similar small signal transconductance for the 0.33 and 0.48μm is consistent with the measured dc transconductance. Regardless of gatelength, the devices exhibit similar output conductance as shown. The bias dependent gate-to-source and gate-to-drain capacitance are shown in Figure F.2. As the gatelength is increased, the gate capacitance proportionately increases.

(see next page for figures)

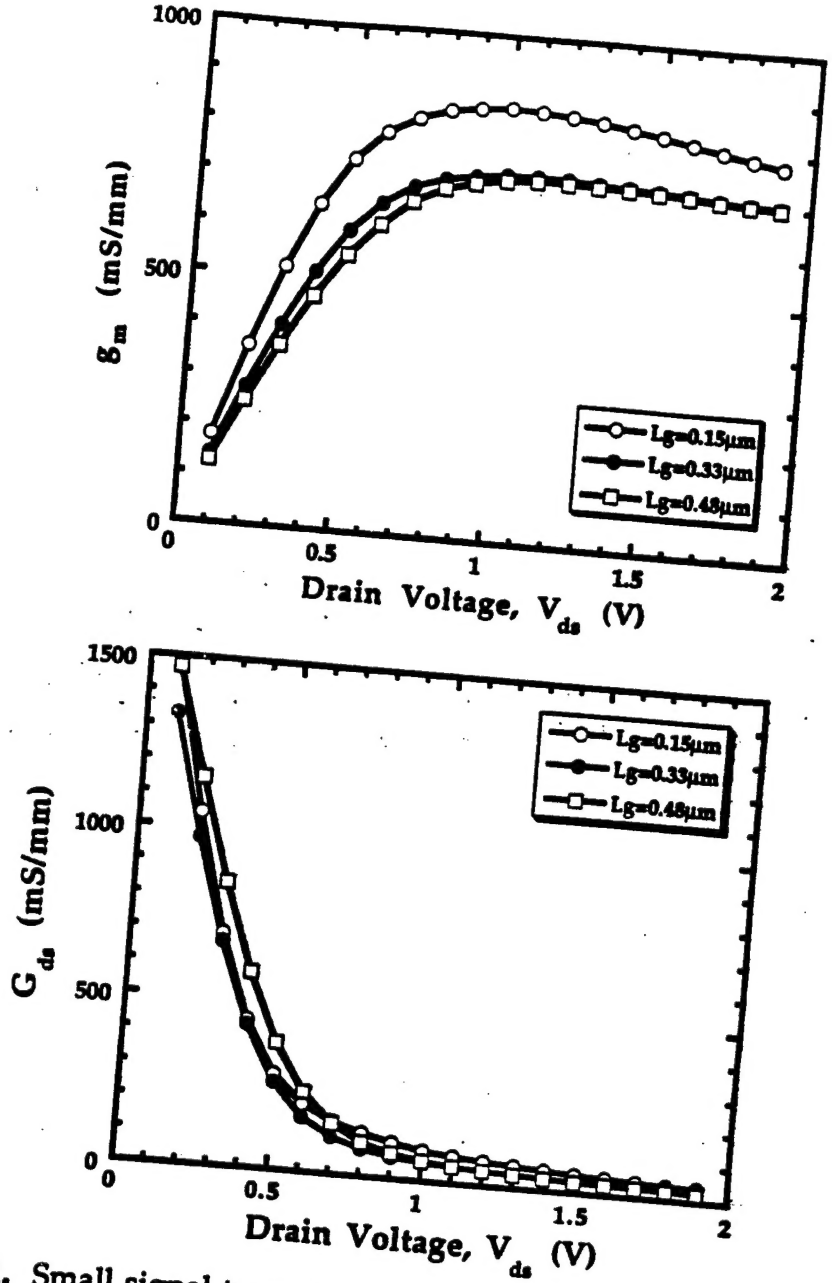


Figure F1. Small signal transconductance (top) and output conductance (bottom) versus drain voltage for various gatelengths.

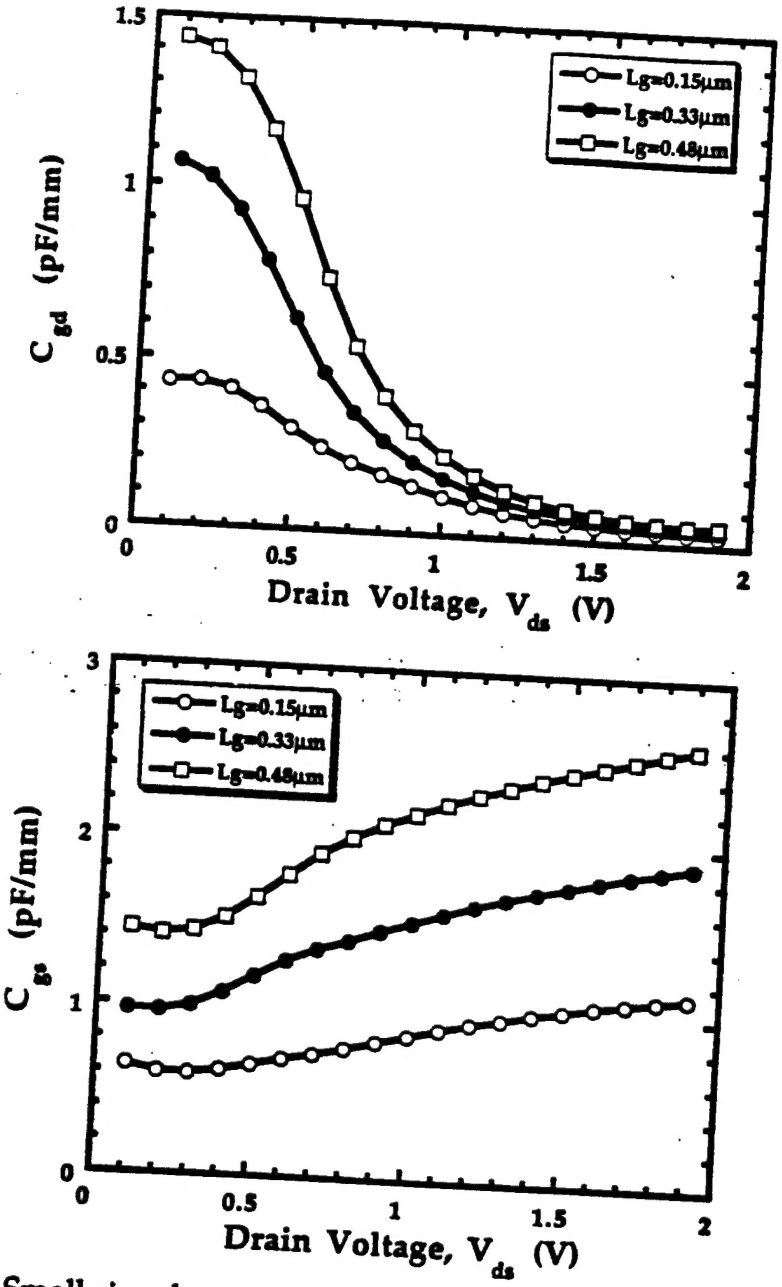


Figure F2. Small signal gate-to-drain capacitance (top) and gate-to-source capacitance (bottom) versus drain voltage for various gatelengths.